

DB2012UIB

Wideband PLC DB2012UIB Module Specification 1.0.1

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U.S. Patent No. x,xxx,xxx, y,yyy,yyy. Canadian Patent No. xx,xxx,xxx, and so on. Other relevant patent grants may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
1.0.0	2016.11.29	Initial version
1.0.1	2016.12.07	Change "HPAV" to "HPGP"

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1 OVERVIEW

The Wideband PLC DB2012UIB Module delivers a set of hardware module, software and service solution to device manufacturers who want their customers to connect domestic electrical appliances, sensores, switches to internet; connect outdoor industrial device to management and controlling center via power-line.

The wideband platform offers:

- The turnkey Modules
- Firmware, which includes mesh network.

2 INTRODUCTION

The DB2012UIB module provides another communication channel to manage the future IOE network.

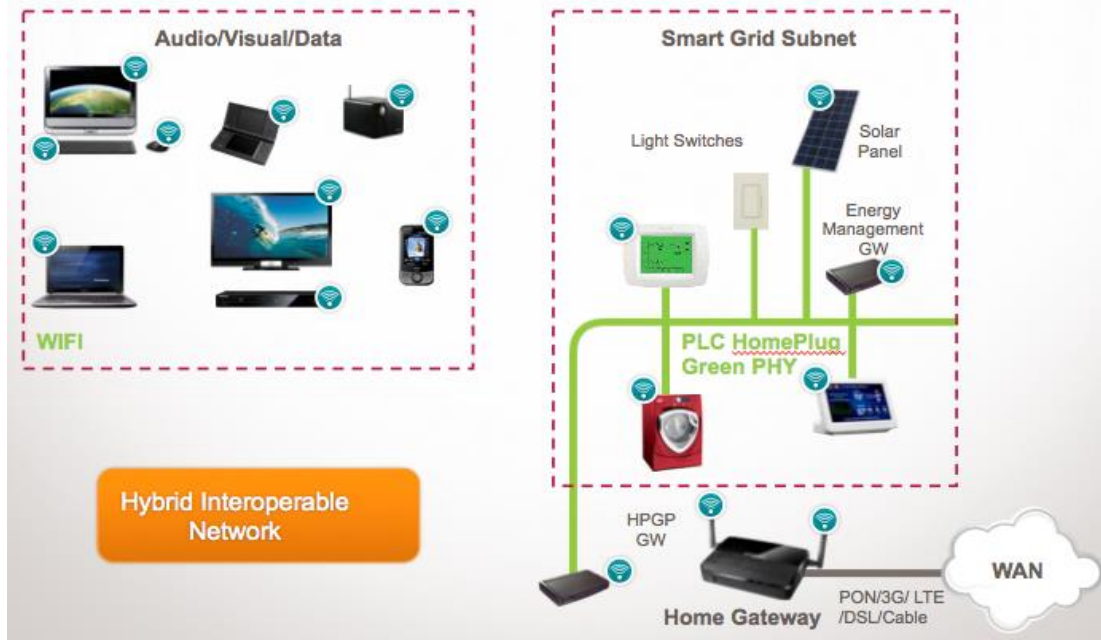


Figure 1: Hybrid Interoperable Network

2.1 HPGP PLC Mesh Network

HPGP PLC offers a unique means of communication for a power-supply system, which takes full advantage of the wide coverage of power-line installations without having to lay dedicated cables. With mesh networking, HPGP devices can exchange data with HPGP gateway, which adapts the HPGP protocol with WIFI, within its network of control. The total 253 HPGP could be connected by HPGP/WIFI adapter.

HPGP Features:

- Spectrum: 2-30MHz
- Modulation: OFDM
- Subcarriers: 917
- Subcarrier Space: 24.414KHz

2.2 DB2012UIB Module

The DB2012UIB Module is a cost-effective, turnkey hardware and software solution designed to connect the home network.

■ DB2012UIB

Based on industry-leading Qualcomm Atheros, Inc. HPGP chip QCA7000, the DB2012UIB is a cost-effective PLC module designed for Home network applications.

3 DB2012UIB MODULE

3.1 General

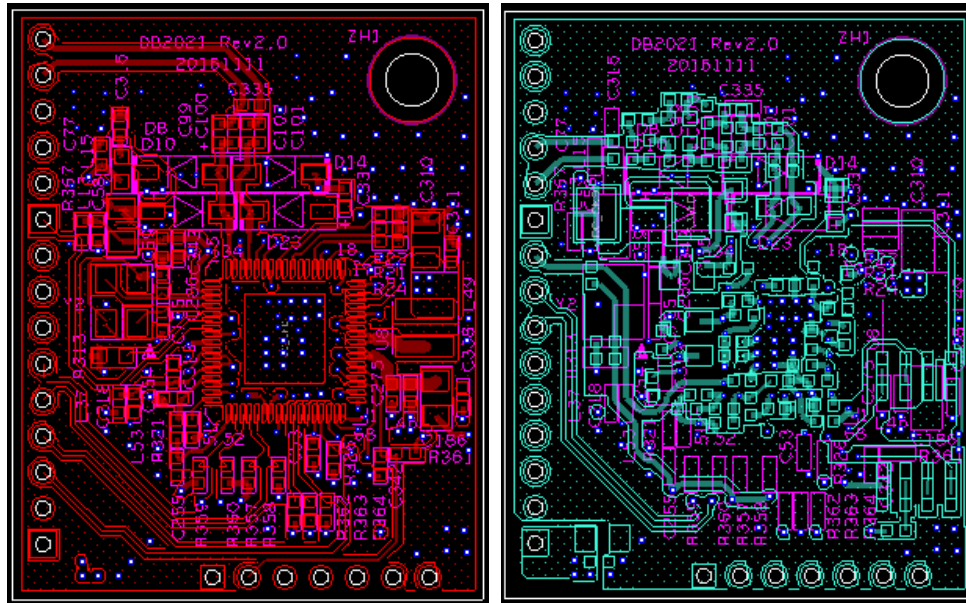


Figure 2: DB2012UIB Board Assembly (Top view and Bottom view)

Feature:

- HPGP chip: QCA7000
- 26.18mm*32.8mm, 4-layer design
- Power-line interface: pin 【10...15】 of 15 pin DIP connector J1 for power line coupling transformer
- Digital interface: pin 【1...4】 of 15 pin DIP connector J1 for GPIO and power. 7 pin DIP connector J3 for UART.

3.2 Block Diagram

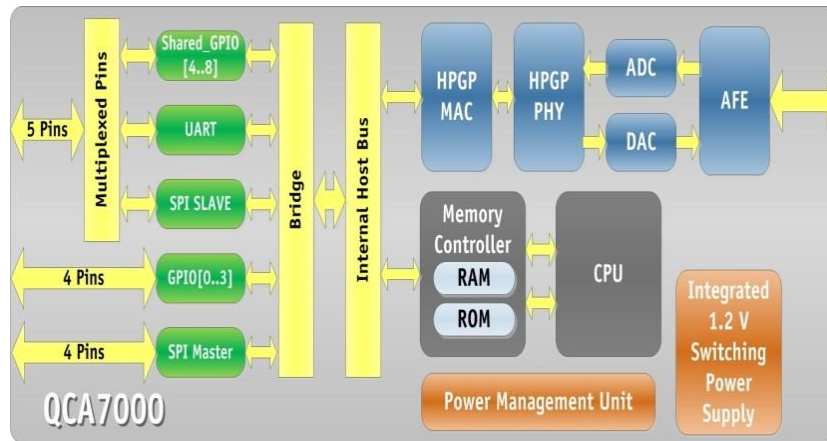


Figure 3: QCA7000

3.3 Pin Definitions

The J1 interface [15*1 Pin Header, 2.0mm] :

Pin	Name	Usage
1	3.3VD	Power Supply, input;
2	GND	Module Ground
3	GPIO[3]	Input, Push button.
4	GPIO[2]	General GPIO for Output/Input, 3.3v TTL.
5	NC	NC, Floating
6	NC	NC, Floating
7	NC	NC, Floating
8	NC	NC, Floating
9	NC	NC, Floating
10	ZC_IN	Power Line Zero Cross in.



		Note: The QCA7000 has an analog amplifier circuit that detects when the 50 Hz or 60 Hz AC power line voltage crosses through zero volts. This input pin is self-biased so it is AC coupled by a capacitor. This input only requires a small AC waveform of about 100mVpp.
11	RX+	Power Line Coupling Transformer Rx+
12	RX-	Power Line Coupling Transformer Rx-
13	GND	Module Ground
14	TX+	Power Line Coupling Transformer Tx+
15	TX-	Power Line Coupling Transformer Tx-

The J3 interface [7*1 Pin Header, 2.0mm] :

Pin	Name	Usage
1	GND	Module Ground
2	/RST	Reset
3	SERIAL_IN	Serial In & UART RXD
4	SERIAL_OUT	Serial Out & UART TXD
5	SERIAL_CS	Serial CS
6	SERIAL_CLK	Serial CLK
7	SERIAL_INT	Serial Int



3.4 Form Factors

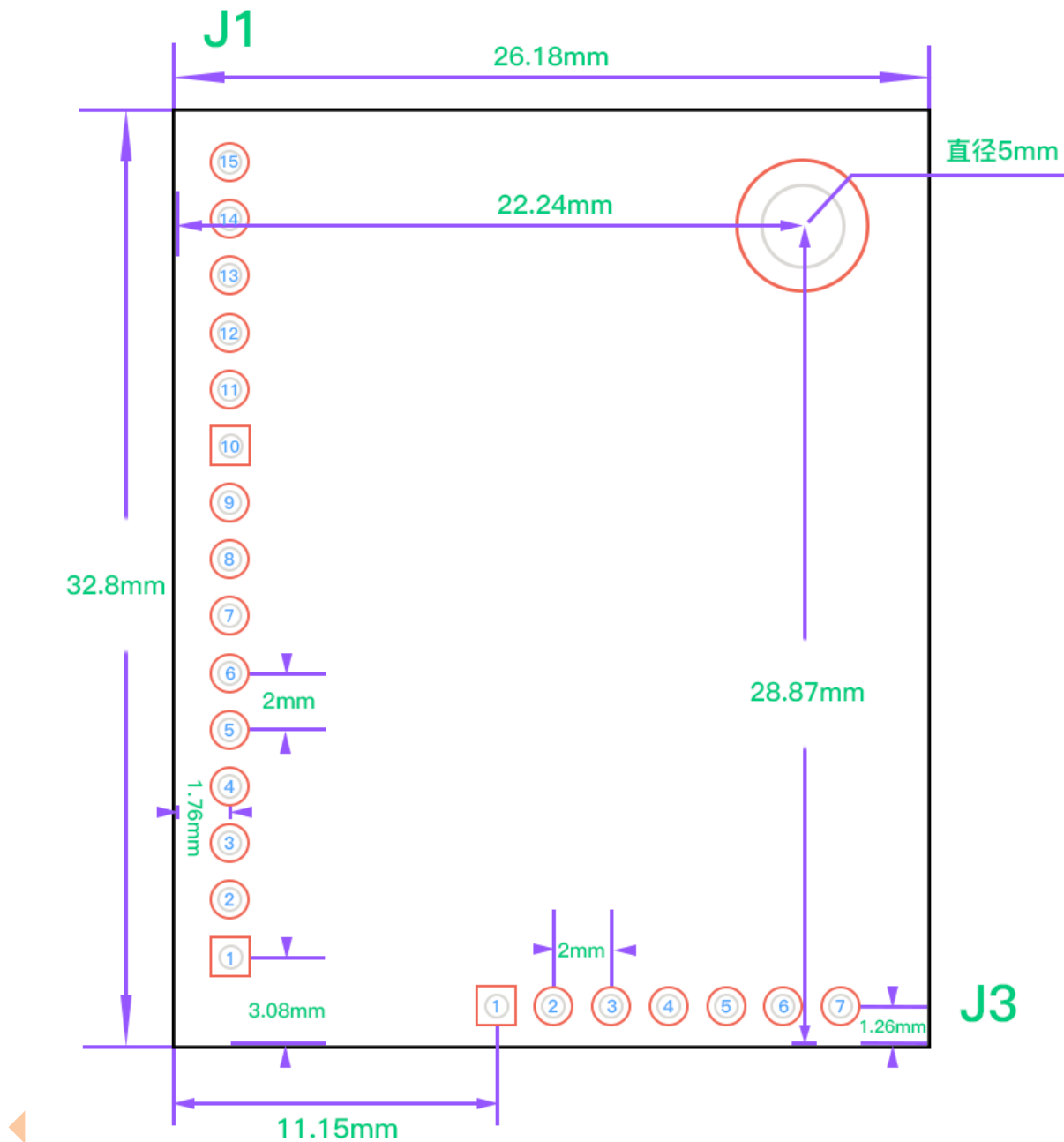


Figure 4: Form Factors

APPENDIX A

A.1 GPIO pin strapping at Power-ON

- Do not connect any GPIO directly to ground or to the 3.3 V bus. After the RESET_L signal goes high FW may drive any GPIO pin to an output. Any pin may be driven high or low by FW to indicate system status using the LED outputs.

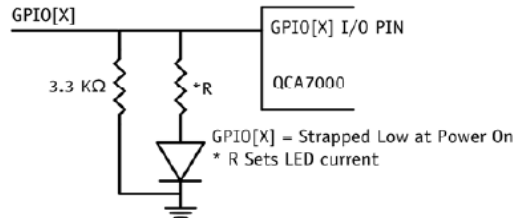


Figure 2-5 QCA7000 Pull-Down LED Strapping

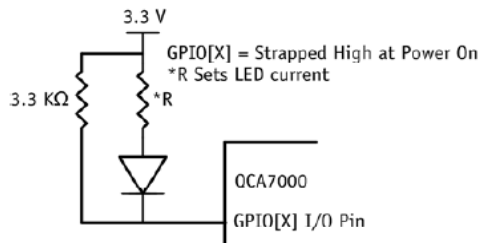


Figure 2-6 QCA7000 Pull-Up LED Strapping

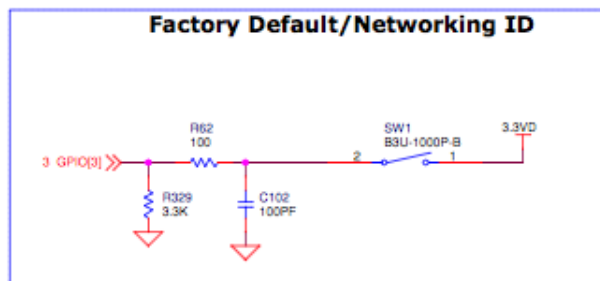
The following additional straps are also available in any mode of operation:

Table 2-4 Special Straps for Test

Symbol	Pin	Strap=1	Strap=0
PLL-Bypass	44	Used for test. 1 = disable the PLL	Normal mode. PD (0) internally

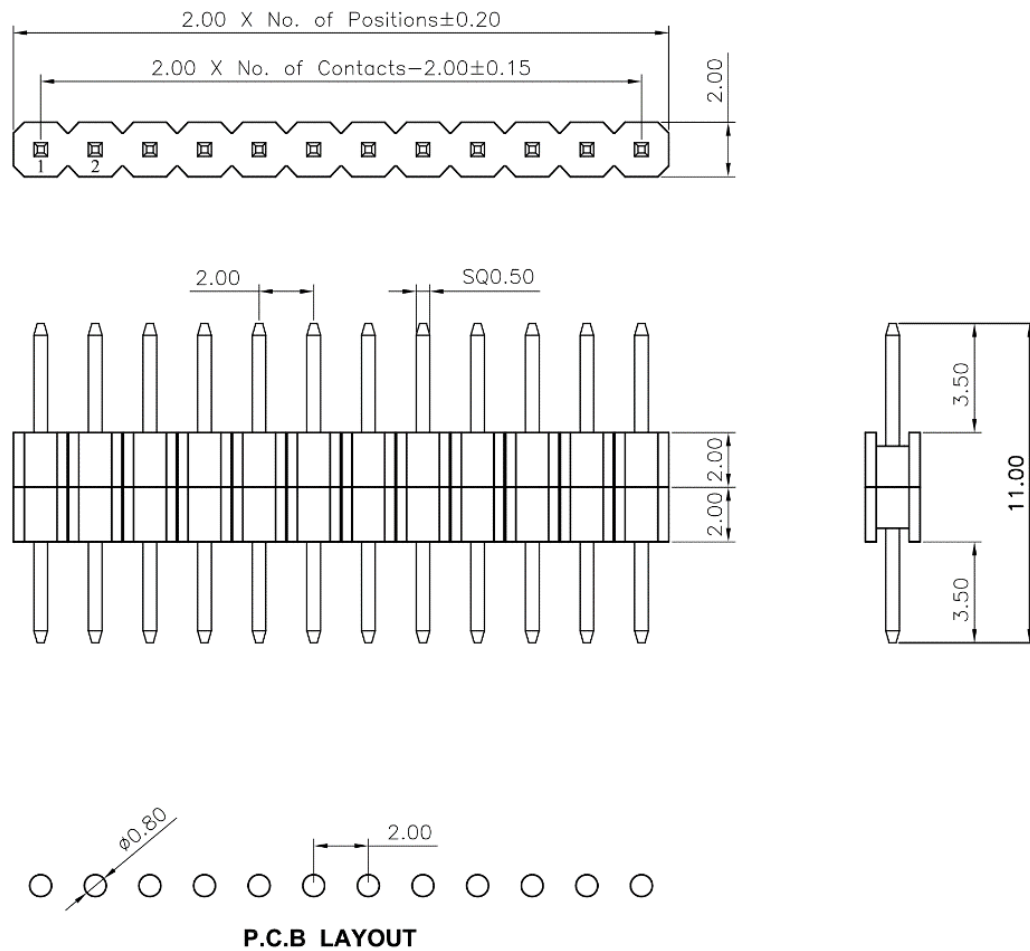
Special test conditions are enabled by the pin straps listed in [Table 2-4](#).

A.2 Push Button Circuit



APPENDIX B

B.1 Connector J1/J3 Definition



J1: Pin Number is 15.

J3: Pin Number is 7.