LT9721 --- Product Brief

MIPI DSI/HDMI to DP with Type-C

Features

- **Single-Port MIPI® DSI Receiver**
  - Compliant with D-PHY1.1 and DSI1.02
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - 80Mb/s~1.5Gb/s per Data Lane
  - Data Lane and Polarity Swapping
  - Internal Rterm Calibration with Less than 5% Error
  - Programmable Equalization
  - Only Non-Burst Mode Supported
  - Support up to 24-bit RGB/YUV Data Format
  - Support YUV4:2:0 Video Format
- **HDMI1.4 Receiver**
  - Compliant to HDMI1.4 Standard
  - Support 3D Video Data Stream
  - Support HDCP1.4 and DDC Slave for EDID
  - Support HDMI2.0 YUV4:2:0 Video Format
  - Support Resolution up to 4Kx2K@30Hz for RGB and 4Kx2K@60Hz for YUV4:2:0
  - Support Hot-Plug Detect
  - Support Status and Control Data Channel (SCDC)
  - No HEAC and CEC Support
- **DP1.2 Transmitter**
  - Compliant to VESA DP1.2 Standard
  - Support Four Lanes with 1.62Gbps (RBR), 2.7Gbps (HBR) or 5.4Gbps (HBR2) Data Rate
  - Data Lane and Polarity Swapping
  - Support HDCP1.3 Encryption
  - Support 18/24-bit RGB and YUV4:2:0 Data Format
  - Build-in Pattern Generation
  - Support Hot-Plug Detect
  - Support Backlight Control for Screen Application
  - Optional SSC 0.5% Down-Spreading Output
  - Configurable and Power-on-Calibrated Output Swing for Optimized EMI
  - Internal Rterm Calibration with Less than 5% Error
- **USB Type-C**
  - Compatible with USB3.1 Gen1, USB Type-C R1.0, DP Alt Mode V1.0 and USB PD R2.0
  - 3 Data Roles Supported: DFP, UFP and DRP
  - 2 Power Roles Supported: Source and Sink
  - USB PD-PHY (Tx/Rx) and BMC Encoding / Decoding
  - USB PD Protocol Control by Software
  - Bi-directional Differential Passive Switch for USB3.1 Gen1 SS signal with less than 2.5-dB Insertion Loss, Controlled by Internal or External CC logic module
  - USB Full-Featured, Orientation and Role Detection
  - 3-level Current Ability Advertise (Host Mode) or Detection (Device Mode) for Type-C Power: USB Default, 1.5A@5V, 3A@5V
  - SBU Data Path Control for DP Alt Mode
  - OCP Control for External VBUS Power Switch
  - Dead Battery Supports (Sink Mode) When No Power Applied
- **Audio Input**
  - Support SPDIF and up to 8-CH I2S Audio Input in MIPI mode
- **Miscellaneous**
  - 1.8V/3.3V Dual Supply Power
  - External 25MHz Rrystal Reference Clock
  - Temperature Range: -40^{0}C ~ +85^{0}C
  - Packaged in 5mm x 5mm BGA81 and 7.5mm x 7.5mm QFN64

Description

The Lontium LT9721 is MIPI/HDMI to DP converter with internal Type-C Alternate Mode switch and PD controller.

For MIPI DSI® input, LT9721 features a single-port MIPI DSI receiver with 1 clock lane and 4 data lanes operating at maximum 1.5Gbps per data lane and a maximum input bandwidth of 6Gbps. The converter decodes the input 18/24-bit RGB packets and converts the formatted video data stream to a 4-lane DP1.2 compliant output, supporting RBR(1.62Gbps), HBR(2.7Gbps) and HBR2(5.4Gbps) link speeds. The build-in optional SSC function reduces EMI effect on EMI-concerned system application.

For HDMI input, LT9721 features a HDMI1.4 receiver with 1 clock lane and 3 data lanes

operating at maximum 3.4Gbps per data lane and a maximum input bandwidth of 10.2Gbps, allowing resolution up to 4Kx2K@30Hz for RGB format and 4Kx2K@60Hz for YUV420 format. The converter also integrates a DDC controller and supports HDCP1.4.

In order to be adaptable to the latest USB Type-C ecosystem, LT9721 integrates a high performance bi-directional passive differential switch controlled by CC logic and PD management unit to releive mobile system design complexity and BOM cost. The switch function is compliant with VESA DP Alternate Mode on USB Type-C Standard.

The LT9721 is fabricated in advanced CMOS process and implemented in a small outline 5mm x 5mm BGA81 (LT9721-B81) and 7.5mm x 7.5mm QFN64 (LT9721-Q64) package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

Application

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

Block Diagram

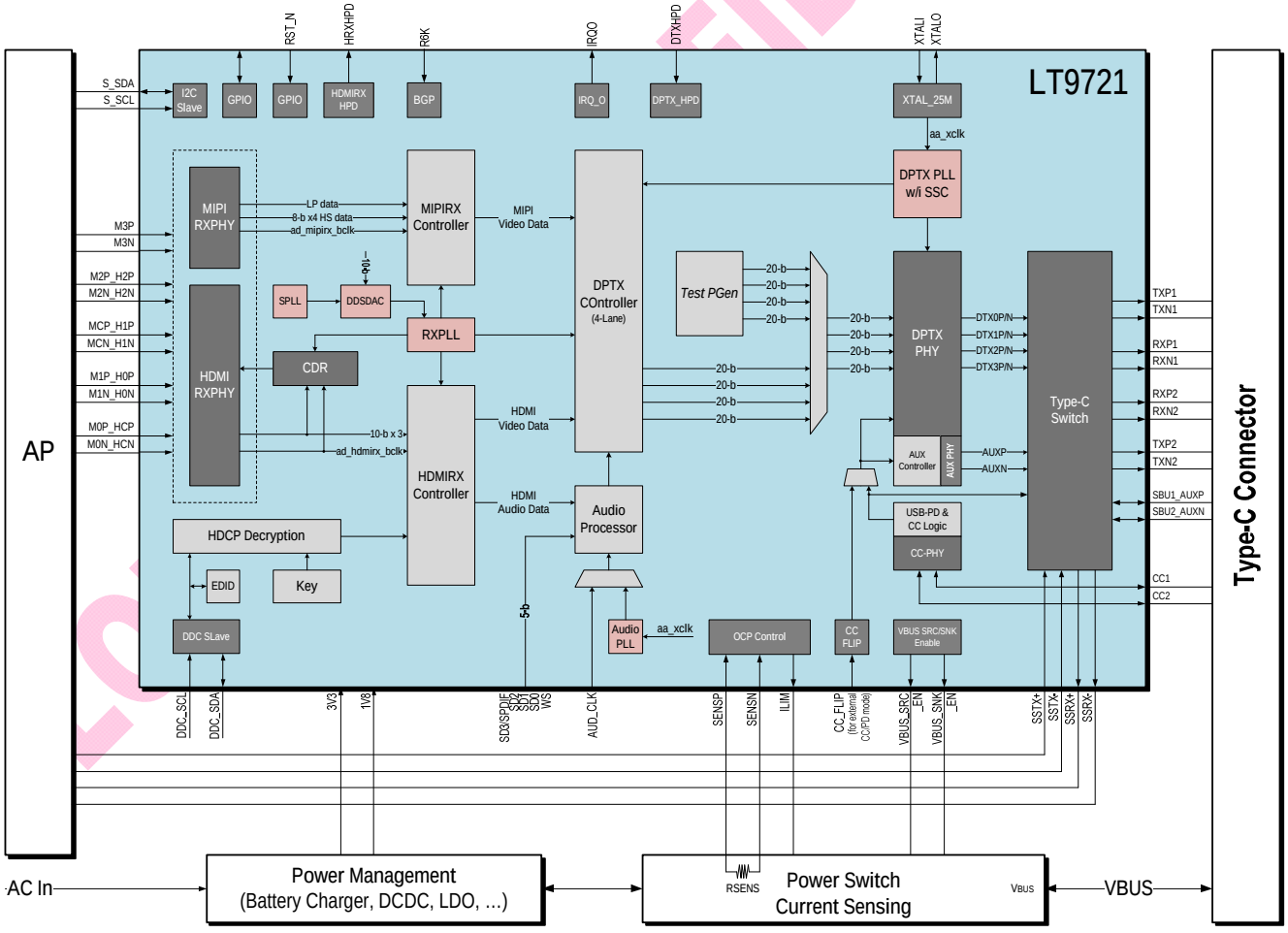
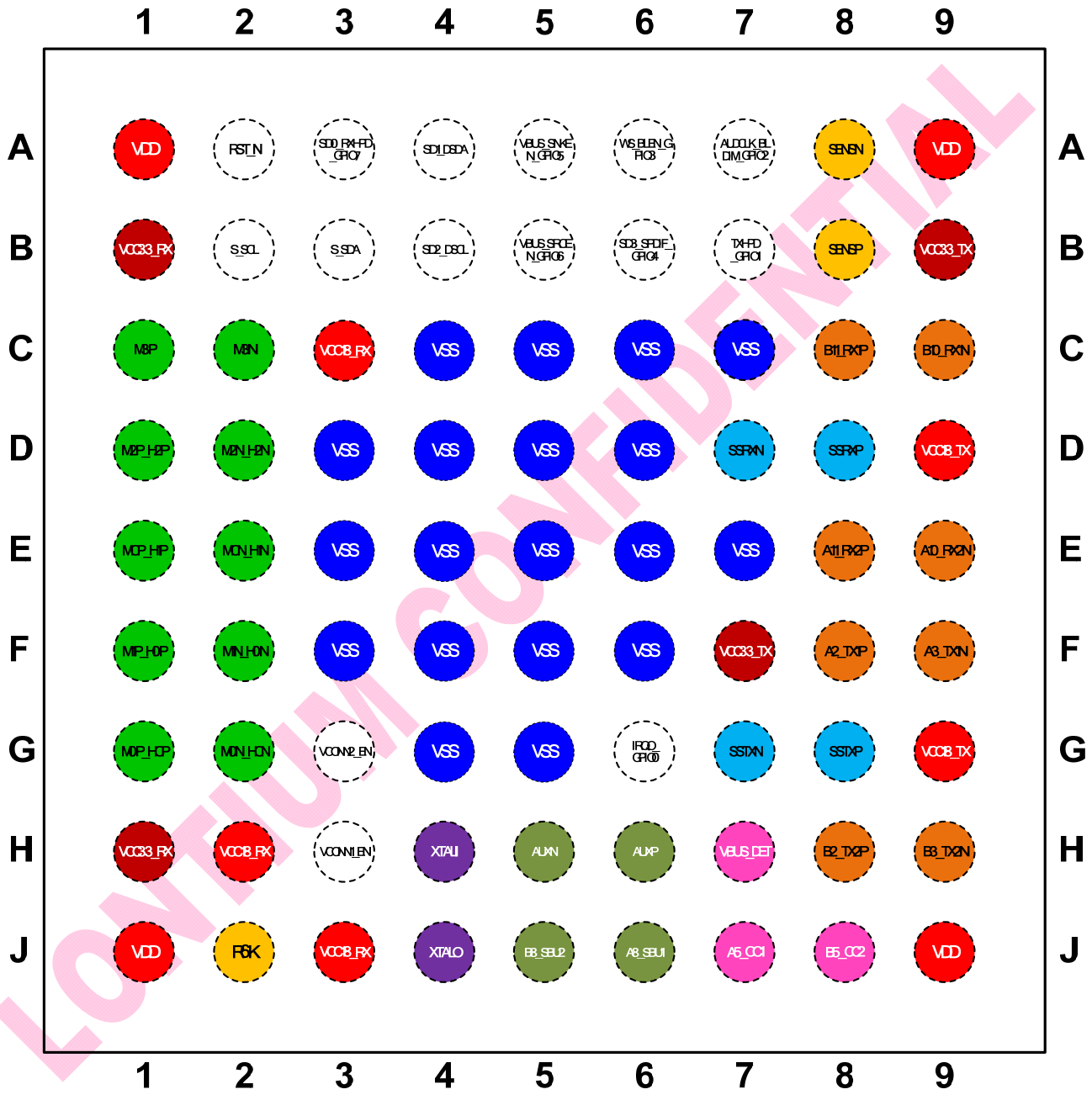


Fig1 Typical Application and System Diagrams

Ball Diagram



Ball Definition

Ball No.	Ball Name	Ball Description
C4,C5,C6,C7,D3, D4,D5,D6,E3,E4, E5,E6,E7,F3,F4, F5,F6,G4,G5	VSS	1.8V Ground 1.8V ground digital core
B1,H1	VCC33_RX	Analog 3.3V Power 3.3V power for analog
C3,H2,J3	VCC18_RX	Analog 1.8V Power 1.8V power for analog
A1,A9,J1,J9	VDD	Digital core 1.8V Power 1.8V power for digital core
B9,F7	VCC33_TX	Analog 3.3V Power 3.3V power for analog
D9,G9	VCC18_TX	Analog 1.8V Power 1.8V power for analog
C2	M3N	MIPI® D-PHY Data Lane-3 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
C1	M3P	MIPI® D-PHY Data Lane-3 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
D2	M2N_H2N	MIPI® D-PHY Data Lane-2 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-2 Positive Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.
D1	M2P_H2P	MIPI® D-PHY Data Lane-2 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-2 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
E2	MCN_H1N	MIPI® D-PHY Clock Lane Negative Input MIPIRX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals HDMIRX Data Lane-1 Negative Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.

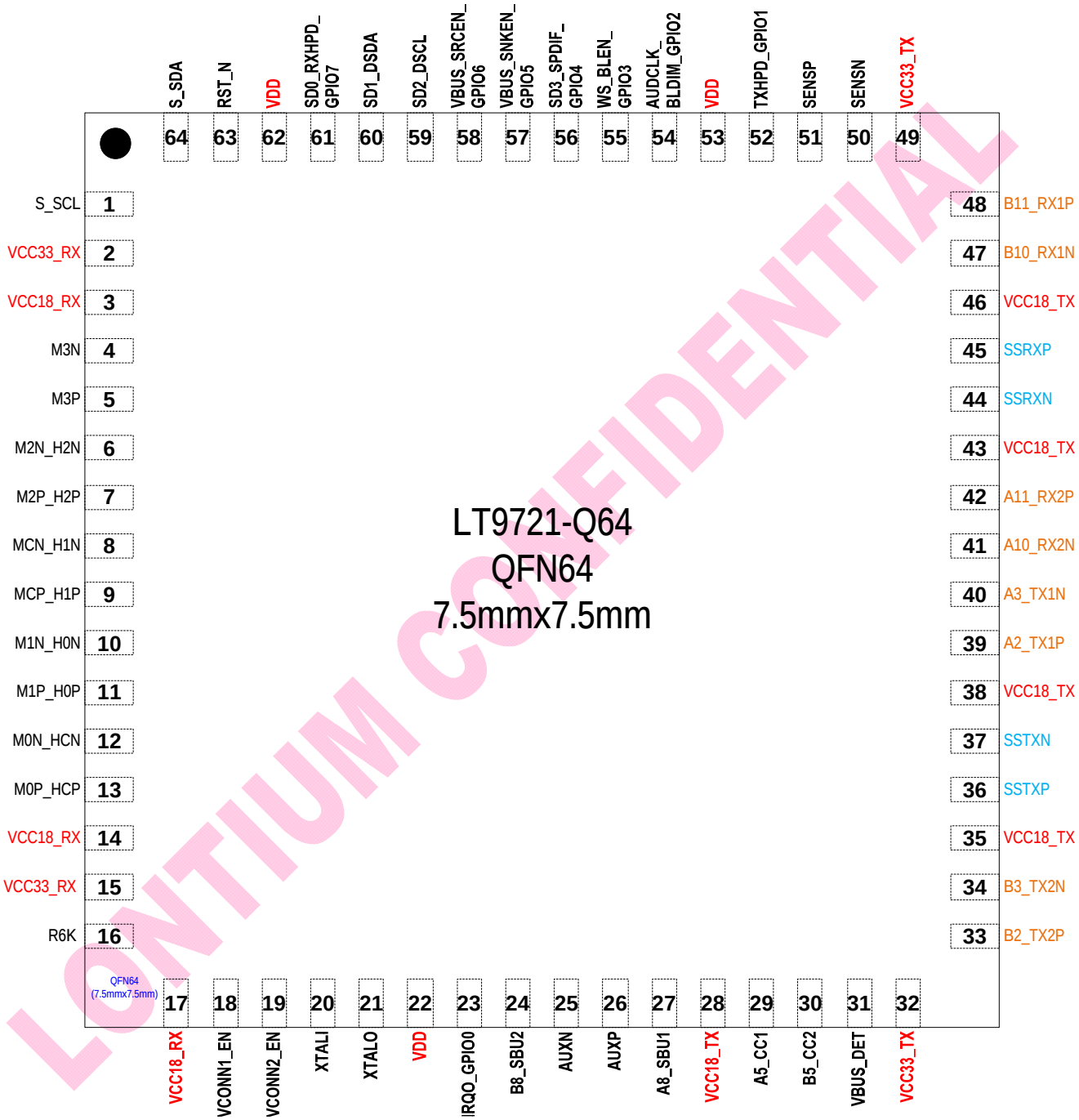
Ball No.	Ball Name	Ball Description
E1	MCP_H1P	MIPI® D-PHY Clock Lane Positive Input MIPIRX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals HDMIRX Data Lane-1 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
F2	M1N_H0N	MIPI® D-PHY Data Lane-1 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-0 Positive Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.
F1	M1P_H0P	MIPI® D-PHY Data Lane-1 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-0 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
G2	M0N_HCN	MIPI® D-PHY Data Lane-0 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Clock Lane Negative Input HDMIRX Negative input of clock differential pairs up to 300MHz.
G1	M0P_HCP	MIPI® D-PHY Data Lane-0 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Clock Lane Positive Input HDMIRX Positive input of clock differential pairs up to 300MHz.
J2	R6K	BandGap External Resistor External 6K resistor for setting internal reference current.
H4	XTALI	Crystal Clock Input A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT9721.
J4	XTALO	Crystal Clock Output A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
H3	VCONN1_EN	TYPE-C VCONN Power Control In default, this pin is configured as GPIO to control an external power switch for VCONN1 on CC1. 5V tolerance.
G3	VCONN2_EN	TYPE-C VCONN Power Control In default, this pin is configured as GPIO to control an external power switch for VCONN2 on CC2. 5V tolerance.
J5	B8_SBU2	TYPE-C SBU2 Sideband Use Channel-2. An AC coupling capacitor is connected between this pin and AUXN.

Ball No.	Ball Name	Ball Description
H5	AUXN	DPTX AUX Channel Negative In/Out Negative in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and B8_SBU2.
H6	AUXP	DPTX AUX Channel Positive In/Out Positive in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and A8_SBU1.
J6	A8_SBU1	TYPE-C SBU1 Sideband Use Channel-1. An AC coupling capacitor is connected between this pin and AUXP.
J7	A5_CC1	TYPE-C Connector Configure Channel-1 TYPE-C CC1 or VCONN1. 5V tolerance.
J8	B5_CC2	TYPE-C Connector Configure Channel-2 TYPE-C CC2 or VCONN2. 5V tolerance.
H7	VBUS_DET	TYPE-C VBUS Power Detect Input VBUS voltage detection input in TYPE-C UFP mode
H8	B2_TX2P	TYPE-C Connector Positive Output TYPE-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
h9	B3_TX2N	TYPE-C Connector Negative Output TYPE-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
G8	SSTXP	USB3.1 Positive Input USB3.1 Gen1 SSTX positive input of differential pairs up to 5.4Gb/s.
G7	SSTXN	USB3.1 Negative Input USB3.1 Gen1 SSRX negative input of differential pairs up to 5.4Gb/s.
F8	A2_TX1P	TYPE-C Connector Positive Output TYPE-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
F9	A3_TX1N	TYPE-C Connector Negative Output TYPE-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
E9	A10_RX2N	TYPE-C Connector Negative Input/Output TYPE-C negative in/out of polarity swappable differential pairs up to 5.4Gb/s.
E8	A11_RX2P	TYPE-C Connector Positive Output TYPE-C positive in/out of polarity swappable differential pairs up to 5.4Gb/s.
D7	SSRXN	USB3.1 Negative Input USB3.1 Gen1 SSRX negative input of differential pairs up to 5.4Gb/s.
D8	SSRXP	USB3.1 Positive Input USB3.1 Gen1 SSRX positive input of differential pairs up to 5.4Gb/s.
C9	B10_RX1N	TYPE-C Connector Negative Input/Output TYPE-C negative in/out of polarity swappable differential pairs up to 5.4Gb/s.

Ball No.	Ball Name	Ball Description
C8	B11_RX1P	TYPE-C Connector Positive Output TYPE-C positive in/out of polarity swappable differential pairs up to 5.4Gb/s.
A8	SENSN	OCP Sense Negative Input Negative sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
B8	SENSP	OCP Sense Positive Input Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
G6	IRQO_GPIO0	Interrupt Request Output In default, this pin is configured as 3.3V interrupt request (IRQ) output. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
B7	TXHPD_GPIO1	DPTX HPD Input DPTX hot-plug detect input Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
A7	AUDCLK_ BLDIM_GPIO2	I2S Clock Input In default, this pin is configured as 1.8/3.3V I2S clock input. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
A6	WS_BLEN_ GPIO3	I2S Audio Word Select Input In default, this pin is configured to 1.8/3.3V I2S channel select input. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
B6	SD3_SPDIF_ GPIO4	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-3. SPDIF Audio Signal Input This pin can also be configured as 1.8/3.3VSPDIF audio data input. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
A5	VBUS_SNKEN _GPIO5	VBUS Sinking Enable Output External VBUS power switch control output in TYPE-C SNK Power Role. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
B5	VBUS_SRCEN _GPIO6	VBUS Sourcing Enable Output External VBUS power switch control output in TYPE-C SRC Power Role. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.

Ball No.	Ball Name	Ball Description
A3	SD0_RXHPD_ GPIO7	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-0. HDMIRX HPD 5V Tolerant Output This pin can also be configured as HDMIRX hot-plug detect output. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
B4	SD2_DSCL	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-2. HDMIRX DDC Clock 5V Tolerant Input This pin can also be configured as DDC serial clock input in HDMIRX mode. 5V tolerance.
A4	SD1_DSDA	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-1. HDMIRX DDC Data 5V Tolerant Input /Output This pin can also be configured as DDC serial data in/out in HDMIRX mode. 5V tolerance.
A2	RST_N	Hardware Reset Input Chip reset signal. Active LOW.
B3	S_SDA	I2C Serial Data Input/Output It serves as the serial port data IO slave for register access. Supports 1.8/3.3V CMOS logic.
B2	S_SCL	I2C Serial Clock Input It serves as the serial port data clock slave for register access. Supports 1.8/3.3V CMOS logic.

Pin Diagram



Pin Definition

Pin No.	Pin Name	Pin Description
1	S_SCL	I2C Serial Clock Input It serves as the serial port data clock slave for register access. Supports 1.8/3.3V CMOS logic.
2	VCC33_RX	Analog 3.3V Power 3.3V power for analog
3	VCC18_RX	Analog 1.8V Power 1.8V power for analog
4	M3N	MIPI® D-PHY Data Lane-3 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
5	M3P	MIPI® D-PHY Data Lane-3 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
6	M2N_H2N	MIPI® D-PHY Data Lane-2 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-2 Positive Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.
7	M2P_H2P	MIPI® D-PHY Data Lane-2 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-2 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
8	MCN_H1N	MIPI® D-PHY Clock Lane Negative Input MIPIRX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals HDMIRX Data Lane-1 Negative Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.
9	MCP_H1P	MIPI® D-PHY Clock Lane Positive Input MIPIRX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals HDMIRX Data Lane-1 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
10	M1N_H0N	MIPI® D-PHY Data Lane-1 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-0 Positive Input HDMIRX Negative input of polarity swappable differential pairs up to 3Gb/s.

Pin No.	Pin Name	Pin Description
11	M1P_H0P	MIPI® D-PHY Data Lane-1 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Data Lane-0 Positive Input HDMIRX Positive input of polarity swappable differential pairs up to 3Gb/s.
12	M0N_HCN	MIPI® D-PHY Data Lane-0 Negative Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Clock Lane Negative Input HDMIRX Negative input of clock differential pairs up to 300MHz.
13	M0P_HCP	MIPI® D-PHY Data Lane-0 Positive Input MIPIRX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. HDMIRX Clock Lane Positive Input HDMIRX Positive input of clock differential pairs up to 300MHz.
14	VCC18_RX	Analog 1.8V Power 1.8V power for analog
15	VCC33_RX	Analog 3.3V Power 3.3V power for analog
16	R6K	BandGap External Resistor External 6K resistor for setting internal reference current.
17	VCC18_RX	Analog 1.8V Power 1.8V power for analog
18	VCONN1_EN	TYPE-C VCONN Power Control In default, this pin is configured as 3.3V GPIO to control an external power switch for VCONN1 on CC1. 5V tolerance.
19	VCONN2_EN	TYPE-C VCONN Power Control In default, this pin is configured as 3.3V GPIO to control an external power switch for VCONN2 on CC2. 5V tolerance.
20	XTALI	Crystal Clock Input A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT9721
21	XTALO	Crystal Clock Output A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
22	VDD	Digital core 1.8V Power 1.8V power for digital core
23	IRQO_GPIO0	Interrupt Request Output In default, this pin is configured as 3.3V interrupt request (IRQ) output. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.

Pin No.	Pin Name	Pin Description
24	B8_SBU2	TYPE-C SBU2 Sideband Use Channel-2. An AC coupling capacitor is connected between this pin and AUXN.
25	AUXN	DPTX AUX Channel Negative In/Out Negative in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and B8_SBU2.
26	AUXP	DPTX AUX Channel Positive In/Out Positive in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and A8_SBU1.
27	A8_SBU1	TYPE-C SBU1 Sideband Use Channel-1. An AC coupling capacitor is connected between this pin and AUXP.
28	VCC18_TX	Analog 1.8V Power 1.8V power for analog.
29	A5_CC1	TYPE-C Connector Configure Channel-1 TYPE-C CC1 or VCONN1. 5V tolerance.
30	B5_CC2	TYPE-C Connector Configure Channel-2 TYPE-C CC2 or VCONN2. 5V tolerance.
31	VBUS_DET	TYPE-C VBUS Power Detect Input VBUS voltage detection input in TYPE-C UFP mode
32	VCC33_TX	Analog 3.3V Power 3.3V power for analog
33	B2_TX2P	TYPE-C Connector Positive Output TYPE-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
34	B3_TX2N	TYPE-C Connector Negative Output TYPE-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
35	VCC18_TX	Analog 1.8V Power 1.8V power for analog.
36	SSTXP	USB3.1 Positive Input USB3.1 Gen1 SSTX positive input of differential pairs up to 5.4Gb/s.
37	SSTXN	USB3.1 Negative Input USB3.1 Gen1 SSRX negative input of differential pairs up to 5.4Gb/s.
38	VCC18_TX	Analog 1.8V Power 1.8V power for analog.
39	A2_TX1P	TYPE-C Connector Positive Output TYPE-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
40	A3_TX1N	TYPE-C Connector Negative Output TYPE-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
41	A10_RX2N	TYPE-C Connector Negative Input/Output TYPE-C negative in/out of polarity swappable differential pairs up to 5.4Gb/s.

Pin No.	Pin Name	Pin Description
42	A11_RX2P	TYPE-C Connector Positive Output TYPE-C positive in/out of polarity swappable differential pairs up to 5.4Gb/s.
43	VCC18_TX	Analog 1.8V Power 1.8V power for analog.
44	SSRXN	USB3.1 Negative Input USB3.1 Gen1 SSRX negative input of differential pairs up to 5.4Gb/s.
45	SSRXP	USB3.1 Positive Input USB3.1 Gen1 SSRX positive input of differential pairs up to 5.4Gb/s.
46	VCC18_TX	Analog 1.8V Power 1.8V power for analog.
47	B10_RX1N	TYPE-C Connector Negative Input/Output TYPE-C negative in/out of polarity swappable differential pairs up to 5.4Gb/s.
48	B11_RX1P	TYPE-C Connector Positive Output TYPE-C positive in/out of polarity swappable differential pairs up to 5.4Gb/s.
49	VCC33_TX	Analog 3.3V Power 3.3V power for analog
50	SENSN	OCP Sense Negative Input Negative sense for external high voltage power path current sense resistance. Short pin to VBUS when unused. 5V tolerance.
51	SENSP	OCP Sense Positive Input Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused. 5V tolerance.
52	TXHPD_GPIO1	DPTX HPD Input DPTX hot-plug detect input Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
53	VDD	Digital core 1.8V Power 1.8V power for digital core
54	AUDCLK_BLDIM_GPIO2	I2S Audio Clock Input In default, this pin is configured as 1.8/3.3V I2S clock input. eDP Backlight Control DIM This pin can also be configured as 3.3V eDP backlight control dim output Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.

Pin No.	Pin Name	Pin Description
55	WS_BLEN_GPIO3	I2S Audio Word Select Input In default, this pin is configured to 1.8/3.3V I2S channel select input. eDP Backlight Control Enable This pin can also be configured as 3.3V eDP backlight control enable output Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
56	SD3_SPDIF_ GPIO4	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-3. SPDIF Audio Signal Input This pin can also be configured as 1.8/3.3V SPDIF audio data input. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
57	VBUS_SNKEN_ GPIO5	VBUS Sinking Enable Output External VBUS power switch control output in TYPE-C SNK Power Role. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
58	VBUS_SRCEN_ GPIO6	VBUS Sourcing Enable Output External VBUS power switch control output in TYPE-C SRC Power Role. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
59	SD2_DSCL	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-2. HDMIRX DDC Clock 5V Tolerant Input This pin can also be configured as DDC serial clock input in HDMIRX mode. 5V tolerance.
60	SD1_DSDA	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-1. HDMIRX DDC Data 5V Tolerant Input /Output This pin can also be configured as DDC serial data in/out in HDMIRX mode. 5V tolerance.
61	SD0_RXHPD_ GPIO7	I2S Serial Audio Data Input In default, this pin is configured to 1.8/3.3V I2S serial audio data input Bit-0. HDMIRX HPD 5V Tolerant Output This pin can also be configured as HDMIRX hot-plug detect output. 5V tolerance. Digital Test Signal Output When this pin is configured as 3.3V GPIO, it serves as digital test signal output.
62	VDD	Digital core 1.8V Power 1.8V power for digital core
63	RST_N	Hardware Reset Input Chip reset signal. Active LOW.

Pin No.	Pin Name	Pin Description
64	S_SDA	I2C Serial Data Input/Output It serves as the serial port data IO slave for register access. Supports 1.8/3.3V CMOS logic.
65	#EPAD	EPAD

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT9721-Q64	-40°C to 85°C	7.5mmx7.5mm QFN64	Tape and Reel
LT9721-B81	-40°C to 85°C	5mmx5mm BGA81	Tape and Reel

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