Product Change Notice

Date of Publication: Jun. 15, 2016
PCN No: PCN20160601
Change Subject: GD25Q128C to GD25Q127C
Change Type: Product Discontinuance
Key Milestones: Last Order Date for GD25Q128C: Mar.30, 2017
Last Ship Date for GD25Q128C: Sep.30, 2017

Impact of Changes and Recommended Actions:

Compared with GD25Q128C, GD25Q127C provides Low power mode and other advanced useful functions. For more detailed information, please refer to the specific datasheet.

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General Feature Comparison:

Feature		GD25Q128C	GD25Q127C
Operating Voltage Range		2.7V -3.6V	2.7V -3.6V
SPI mode		×1, ×2, ×4, QPI	×1, ×2, ×4
Clock Frequency	Fast Read	104MHz	104MHz
	Read	80MHz	80MHz
Operating Temperature		-40 to 85℃	-40 to 85℃
Architecture	Sector	4KB	4KB
	Block	32KB or 64KB	32KB or 64KB
RESET#		Yes	Yes
Data Protection	Secured OTP	Yes	Yes
	Block Protection	BP0,BP1,BP2,BP3,BP4	BP0,BP1,BP2,BP3,BP4
	Top/Bottom Protection	Yes	Yes
	Complementary Protection	Yes	Yes
Package Option	SOP8 208MIL	Yes	Yes
	VSOP8 208MIL	Yes	Yes
	SOP16 300MIL	Yes	Yes
	DIP8 300MIL	Yes	Yes
	WSON8 5x6mm	Yes	Yes
	WSON8 6x8mm	Yes	Yes
	TFBGA24 (6*4 ball array)	Yes	Yes
Power Consumption	Operating Current(Read)@80MHz Q=Open(*1,*2,*4 I/O)	typ 13 mA, max 18 mA	typ 13 mA, max 18 mA
	Operating Current(Read)@104MHz Q=Open(*1 I/O)	typ 15 mA, max 20 mA	typ 15 mA, max 20 mA
Program/Erase Performance	Page Programming Time	typ 0.6 ms, max 2.4 ms	typ 0.6 ms, max 2.4 ms
	Sector Erase Time	typ 50 ms, max 400 ms	typ 50 ms, max 400 ms
	Block Erase Time (32KB)	typ 200 ms, max 1000 ms	typ 200 ms, max 1000 ms
	Block Erase Time (64KB)	typ 300 ms, max 1200 ms	typ 300 ms, max 1200 ms
	Chip Erase Time	typ 60s, max 120 s	typ 60s, max 120 s

Production Status for 65nm HLMC fab GD25Q127C:

Sample Availability	**Jan. 30, 2016**
Mass Production	**May. 30, 2016**