保密等级：公开

HB8102P Remote controller

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1、General Descriptions

The HB8102P IC is a high-performance 4-bit RISC micro-controller embedded with 2KX12 OTP, 32X4 bits SRAM, 12 Input/Output pins, one input pin and built-in one IR LED drive pin. it's flexible and cost-effective solution for remote control of TV, FANS, Air conditioners ... etc.

2、Features

- MCU Operating voltage: 1.8V to 3.6V
- MCU Operation frequency:

(a) Internal 32MHz RC OSC : 250KHz/1MHz/2MHz/4MHz

(b) External 4MHz X'tal OSC : 250KHz/500KHz/1MHz/2MHz

- Memory Size
- □ Program ROM size: 2KX12 bits (OTP type)

SRAM size: 32x4 bits

- Wake up function for power-down mode
- □ HALT mode wake up source: can be wake up from HALT mode to NORMAL mode and executing wake up sub-routine program.
- Provided 12 input /output pins: each I/O has bit programmable as input or output port , these 12 I/Os also provided wake up function and pull up resistors configured by registers.

(a) They are provided with high sink current 20mA @VDD=3V, VOL=0.5V.

(b) They are provided with drive current 7mA @VDD=3V, VOH=2.5V.

(c) Pull up 150k ohm resistor @VDD=3V.

- Provided 1 input pin (PA3), shared with RESETB/VPP pin by option, with pull up 150k ohm resistor @ VDD=3V.
- Built-in one IR LED drive pin.
- (Sink current : I_{OL}=210mA at VDD=3V and V_{OL}=0.3V)
- Provided key scan function in halt mode, power consumption <3uA @VDD=3V, key scan can be enabled/disabled by control register, any of these I/O pins will not act as key scan pin if this I/O's direction is setting as output port, others are setting as input pin , they will execute key scan function.

(a) In HALT mode, if key scan function enabled, power consumption <3uA @VDD=3V.

(b) In HALT mode, if key scan function disabled, power consumption <1uA @VDD=3V.

- One 8 bits timer, clock source of timer is 8MHz/8192 (1KHz), the content of timer can be cleared and read by program.
- Oscillator type by option

(a) External X'tal oscillator 4MHz (external ceramic resonator or crystal oscillator, the pin of X'tal is shared with PB0 and PB1 pin)

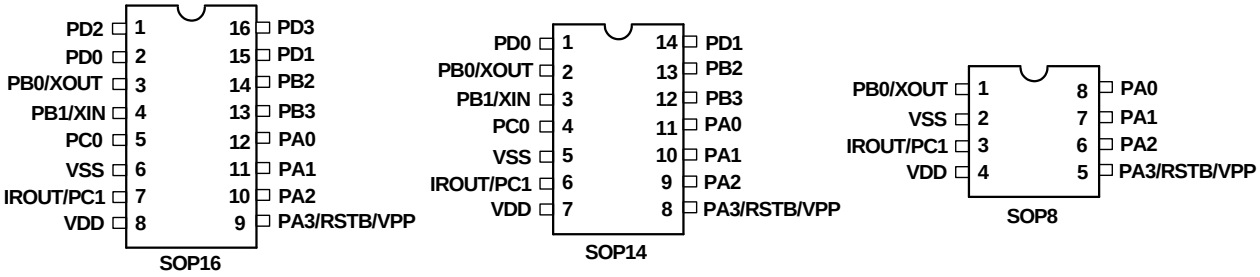
(b) Built-in internal RC OSC 32 MHz

frequency deviation within ±2% VDD=1.8V~3.6V, temp= -20 ºC ~70 ºC

- Four reset condition
- □ Low voltage reset (LVR=1.5V)
- □ Power on RC-reset
- □ External reset (RSTB) pin shared with PA3 by option.
- □ Watch dog timer overflow reset (WDT period is 1 sec)

3、Package SOP14/SOP16 /SOP8

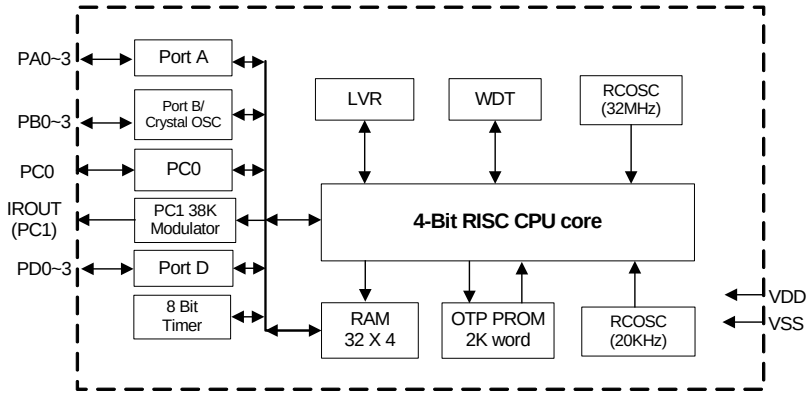
Remote controller



4、Pads Information

PAD Name	Type	State After Reset	Description
Reset/Power Input			
VDD	P	High	Power input pin.
VSS	P	Low	Ground input pin.
General I/O ports			
PA0~PA2	I/O	XXXX	PA0~PA2 are programmable bi-direction pin. Pull up resistor 150k ohm. Edge (rising or falling) trigger function as input mode.
PA3/VPP (RSTB)	I	X	PA3 is a shared pin with external reset RSTB pin by option. Pull up resistor 150k ohm. PA3 is also as VPP pin, no option is needed. Edge (rising or falling) trigger function.
PB0~PB1 (XOUT,XIN)	I/O (O,I)	XX	PB0 and PB1 are programmable bi-direction pin. Pull up resistor 150k ohm. PB1/XIN, PB0/XOUT by option, XIN and XOUT connected to external X'tal 4MHz. Edge (rising or falling) trigger function as input mode.
PB2~PB3	I/O	XXXX	PB2, PB3 is a programmable bi-direction pin. Pull up resistor 150k ohm. Edge (rising or falling) trigger function as input mode.
PC0	I/O	X	PC0 is a programmable bi-direction pin. Pull up resistor 150k ohm. Edge (rising or falling) trigger function as input mode.
IROUT (PC1)	O	X	IROUT is an IR signal output pin. Open drain and high sink current type. IROUT/PC1 is a shared pin, by control register controlled. PC1 is an open drain output port.
PD0~PD3	I/O	XXXX	PD0 ~ PD3 are a programmable Input /Output port. Pull up resistor 150k ohm. Edge (rising or falling) trigger function.

Block Diagram



5、Electrical Characteristics

5.1. Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-40 to 85	ºC
Storage Temperature	T_{STO}	-50 to 150	ºC

5.2.DC/AC Characteristics

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{DD}	-	1.8	-	3.6	V
Operating Current	I_{OP1}	3V , MCU run at 4 MIPS	-	2.2	-	mA
Standby Current	I_{STBY1}	MCU stop, WDT off, key scan off	-	0.1		uA
Standby Current	I_{STBY2}	MCU stop, WDT off, key scan on	-	0.7	3	uA
Input High Level	V_{IH}	All I/O port	$0.8*V_{DD}$	-	-	V
Input Low Level	V_{IL}	All I/O port	-	-	$0.2*V_{DD}$	V
Output Drive	I_{OH}	VDD=3V , V_{OH}=2.5V	-	-7	-	mA
Output Sink	I_{OL1}	VDD=3V , V_{OL}=0.5V	-	20	-	mA
Output Sink	I_{OL2}	VDD=3V , V_{OL}=0.3V	-	210	-	mA
Input Resistor	R_{up}	Pull up 150K ohm	-	150	-	K ohm
LVR	V_{LVR}			1.5		V

AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Internal HRCOSC Frequency	F_{OSC1}	VDD=1.8SV~3.6V Temp.= 25ºC	31.36	32±2%	32.64	MHz
External EXTOSC	F_{XTAL}	VDD=1.8V~3.6V		1~4		MHz
MCU Operation frequency	F_{MCU1}	VDD=1.8V~3.6V		4MHz/2MHz/1MHz/250KHz		MHz
MCU Operation voltage	V_{MCU}		1.8	3.0	3.6	V
Internal LRCOSC Frequency	F_{LOSC}	VDD=3V		20KHz±50%		KHz
WDT period	T_{WDT}	VDD=1.8V~3.6V		1		Sec
Stable clock delay after HRCOSC clock	CKstable1	(Note 1)	-	320us +1024 x (1/ FMCK) (Note 2)		us
Stable clock delay after wake	CKstable2	(Note 3)		1024 x (1/ FMCK) (Note 2)		us

Note1: The stable clock delay is place after first clock output of HRCOSC or external X'tal before user's first instruction, it means the user's program will get more stable clock after power on reset.

Note2: F_{MCK} = MCU operating clock

Note3: The stable clock delay (CKstable2) is place after first clock output of HRCOSC or external X'tal before user's first instruction, it means the user's program will get more stable clock after wake up.

6、Functional Description

This MCU inside HB8102P is a high performance process, and operation frequency could be from 250KHz up to 8MHz depending on the application.

6.1. Program ROM (PROM)

HB8102P supports 2K words OTP ROM, the address for ROM is located on $000H ~ $7FFH, address $000H ~ $$5FFh stores execution program and system area, and the last 512 location (except address $640h ~ $66Fh) is reserved area for testing program. The user shall not use this area in any case. Assembler shall check user program on this limitation. Hardware does not need to check this restriction. PROM is divided into two parts, one is user program area (address $000 ~ $5FFh), and address $640h ~ $66Fh is for data storing only, it can be read in any mode even in locked mode.

Address	Description
000h ~ 0FFh	User area (1.5KX12)
100h ~ 1FFh	
200h ~ 2FFh	
…..	
500h ~ 5FFh	
600h ~ 63Fh	Reserved area
640h ~ 66Fh	user area(48X12), only for data storing only, don't use to storing program
670h ~ 7FFh	Reserved area

Note: The content of OTP ROM address $640h~$66Fh can be read by program which using DMDL, DMDM and DMDH registers. The address $600h~$63Fh, $670h~$7FFh can't be read by program.

Read PROM data is addressed by the DMA2~DMA0 three registers which address range is located in $000H ~ $5FFH and $640H~$66FH. After these registers (DMA0~2) are specified by firmware, the 12bits. data of PROM can be moved to A register by three times, they are LD A, (DMDL) LD A, (DMDM) and LD A, (DMDH).

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA3 three registers built a 11 bit addressing space for read PROM data, DMA0 is lowest nibble address, DMA2 is highest nibble address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	X	DMA2.2	DMA2.1	DMA2.0	
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data of program ROM by address DMA0 ~ DMA2. Writing Ah to this register will turn off option mode, write AH again will turn on option mode.(only for test prog.)
DMDM	1DH	R	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	DMDM is used to read middle nibble data from program ROM by address DMA0 ~ DMA2. Writing this register with data 05h will clear watch dog timer (WDT)
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read the high nibble data program ROM by address DMA0~DMA2

For example, assume that ROM (356H) = 587H.

```
LD A, #3
LD (DMA2), A
LD A, #5
LD (DMA1), A
LD A, #6
LD (DMA0), A       ; PROM address = 356H
LD A, (DMDL)       ; A register = 7H ; low nibble data of PROM address 356H
LD A, (DMDM)       ; A register = 8H; middle nibble data of PROM address 356H
LD A, (DMDH)       ; A register = 5H; high nibble data of PROM address 356H
```

6.2. SRAM and I/O Memory Map

HB8102P provided 32 nibbles SRAM on the locations $20H~$3FH, these address of SRAM is different from PROM's address.

Direct Addressing (use MAH)		Real SRAM Address	SRAM MAP
MAH=XH (MAH no effect)	00H~1FH		Common I/O port and SFR(special function register) register
MAH=0H	20H~3FH	00H~1FH	USER SRAM (32x4)

6.2.1. I/O Memory Map

The I/O memory map consists of common I/O and extended I/O. These I/O provide some data operation instructions as the following

6.2.2. Common I/O

The previously described common block is defined as the common I/O block. A common I/O provided LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP operation. Bit set/clear can only be operated on the address range from 00H to 0FH, except indirect operation is used.

U: unchanged X: unknown value;R/W: readable & writeable;R: readable only;W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	0	0	CF	ZF	ZF : Zero status register CF : Carry status register
Reserved	01H	R/W	xxxx	X	X	X	X	Reserved
IOC_PA	02H	R/W	0	USER 0	IOCA2	IOCA1	IOCA0	IOCA0~IOCA2: control Port A I/O direction. 1: set PA0~PA2 as output port. 0: set PA0~PA2 as input port of corresponding PA0~PA2 bit USER0: 1 bit user RAM
DATA_PA	03H	R/W	xxxx	DPA3(Read only)	DPA2	DPA1	DPA0	Read Port A data from PA0~PA3 port and write data to PA0~PA2 (I/O direction is defined by IOC_PA register)
PC_CTRL	04H	R/W	xxxx	PC0PU	PC0WK	IOCPC0	DPC0(R/W)	DPC0(PC0 PIN) is an bi-direction I/O port. IOCPC0: control PC0 IO direction. 1: set PC0 as output port. 0: set PC0 as input port PC0WK: wake up enable control 0: PC0 wake up disabled 1: PC0 wake up enabled PC0PU: control PC0 pull up resistor. 0: PC0 pull up resistor disabled 1: PC0 pull up resistor enabled

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
IOC_PB	05H	R/W	0	IOCB3	IOCB2	IOCB1	IOCB0	IOCB0~IOCB3: control Port B I/O direction. 1: set PB0~PB3 as output port 0: set PB0~PB3 as input port of corresponding PB0~PB3 bit
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read Port B data from PB0~PB3 port and write to PB0~PB3 (I/O direction is define by IOC_PB register)
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user RAM
Reserved	08H	R/W	xxxx	X	X	X	X	Reserved
Reserved	09H	R/W	xxxx	X	X	X	X	Reserved
Reserved	0AH	R/W	xxxx	X	X	X	X	Reserved
Reserved	0BH	R/W	xxxx	X	X	X	X	Reserved
IOC_PD	0CH	R/W	0	IOCD3	IOCD2	IOCD1	IOCD0	IOCD0~IOCD3: control Port D I/O direction. 1: set PD0~PD3 as output port. 0: set PD0~PD3 as input port of corresponding PD0~PD3 bit
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read Port D data from PD0~PD3 port and write to PD0~PD3 (I/O direction is define by IOC_PD register)
SCALER1	0EH	R/W	0	TM1EN	TM1IFG	T1DIV1	T1DIV0	T1DIV1~0T1DIV: The pre-scaler of TIMER1 Timer 1 clock source defined below: F_{MCK} = MCU operating clock T1DIV1 | T1DIV0 | TM1CK 0 | 0 | F_{MCK}/8192 0 | 1 | F_{MCK} /4096 1 | 0 | F_{MCK} /2048 1 | 1 | F_{MCK} /1024 TM1IFG: Timer 1 overflow flag 0: no overflow was occurred. 1: overflow was occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user RAM
TIM1_L	11H	R	0	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
IR_DIV	13H	R/W	0	DPC1 (IROUT)	IRDIV2	IRDIV1	IRDIV0	DPC1(PC1/IROUT) is an output port for IR LED driving.IRDIV2~IRDIV0: define outputfrequency and duty of IROUT pin
Reserved	14H~17H							Reserved
MA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA3 three registers built a 11 bits addressing space for read PROM data, DMA0 is lowest nibble address, DMA2 is highest nibble address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	x	DMA2.2	DMA2.1	DMA2.0	
Reserved	1BH	x	xxxx	x	x	x	x	Reserved
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data of program ROM by address DMA0 ~ DMA2. Writing Ah to this register will turn off option mode, write AH again will turn on option mode.(only for test prog.)
DMDM	1DH	R	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	DMDM is used to read middle nibble data from program ROM by address DMA0 ~ DMA2. Writing this register with data 05h will clear watch dog timer (WDT)
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read the high nibble data program ROM by address DMA0~DMA2
Reserved	1FH	W/R	xxxx	X	X	X	X	Reserved
USER SRAM 32 nibbles	20H~3FH	R/W	xxxx	SRAM.3	SRAM.2	SRAM.1	SRAM.0	

6.2.3. Extended I/O

To extend I/O memory space, HB8102P provided two special instructions, “LD A, **EXIO**(n)” and “LD **EXIO**(n), A”, where n = 00H ~ 0FH” to obtain the 16 extra I/O registers. These registers are used for the I/O port pull up resistors control and wake up control, they can be accessed by two “LD” data transfer instruction only. For example, the pull up resistor of port A is enabled, the program as shown below.

LD A, #FH

LD **EXIO**(00H), A

U: unchanged X: unknown value R/W: readable&writeable R: readable only W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
Reserved	01H	X	xxxx	X	X	X	X	Reserved
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
Reserved	03H	X	xxxx	X	X	X	X	Reserved
PDPU	04H	W	0000	PDPU.3	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
Reserved	05H	X	xxxx	X	X	X	X	Reserved
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled
PDWK	08H	W	0000	PDWK.3	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled
Reserved	09H~0FH							Reserved

6.3. Halt Mode & Wake up

The MCU is changed into HALT mode (MCU clock and HRCOSC stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3, PD0~PD3 and PC0 are provided the wake up function when rising edge or falling edge trigger was occurred in halt mode. The program counter will be changed to $004H when HALT instruction executed immediately, and program counter will go to next address after stable time delay (CKstable1, see page 4) while wake up condition was occurred. “system resetb” signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will be changed from $004h to $000h, program counter goes to next address after stable time delay (CKstable1, see page 4). Furthermore, the SRAM will keep their previous data without changed in this mode.

6.4. Watch Dog Timer Reset (WDT)

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. This timer can be enabled or disabled by option. WDT will not have any action when WDT disabled. Firmware shall run an "clear watch dog timer" (write data 5h to register $1D) instruction before WDT time out if WDT is enabled. It will generate a reset signal to reset whole system when WDT overflow. The watch dog timer is a simple counter. It's provided only one time-out period 1sec when WDTEN option enabled, and the clock source uses internal HRCOSC oscillator. WDT can works in NORMAL mode but disabled in HALT mode.

WDT will be reset when wake up from halt, after power on reset or firmware cleared by firmware. The reset watch dog timer sequence is as below :

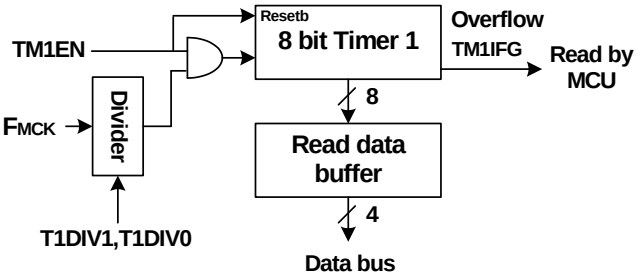
LD A, #05H

LD (1DH), A ; clear watch dog timer

Notice: For avoiding dead lock and system stable, It's strongly recommended don't use more than one "reset watch dog" in program.

6.5. Programable 8 bits TIMER1

The Timer 1 is an 8 bit up timer. The overflow interval can be easy generated by reading the content value of timer 1 and reset values of Timer 1 to 00h by setting TIM1EN=0. The content value of Timer 1 would be readable only by programmer.



Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
TIM1_L	11H	R	0000	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0000	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
SCALER1	0EH	R/W	0000	TM1EN	TM1IFG	T1DIV1	T1DIV0	T1DIV1~0T1DIV: The pre-scaler of TIMER1Timer 1 clock source defined below: FMCK = MCU operating clock T1DIV1 / T1DIV0 / TM1CK 0 / 0 / FMCK/8192 0 / 1 / FMCK /4096 1 / 0 / FMCK /2048 1 / 1 / FMCK /1024 TM1IFG: Timer 1 overflow flag 0: no overflow was occurred. 1: overflow was occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled

The clock source of Timer 1 can come from the frequency divider, there are 4 kinds of clock rate selected by register T1DIV1 and T1DIV0 in this divider, and the divider's clock source is come from MCU operation clock.

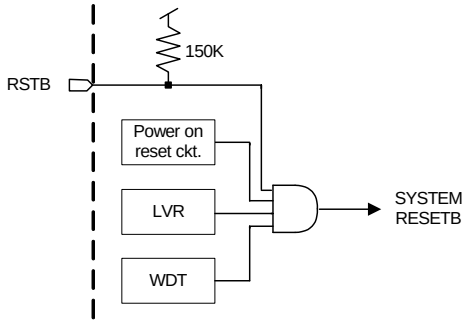
TM1CK= Timer 1 clock source (**F_{MCK}** = MCU operating clock)

T1DIV1	T1DIV0	TM1CK
0	0	F_{MCK} /8192
0	1	F_{MCK} /4096
1	0	F_{MCK} /2048
1	1	F_{MCK} /1024

The 8 bits content of Timer 1 can be reset to 00h by TMI1EN setting to 0, it will be up count while Timer 1 clock source rising after TIM1EN setting to 1. The read operation sequence of TIM1.7~TIM1.0 must be follow low nibble (TIM1_L) first and high nibble (TIM1_H) later. The Timer 1 will issue an overflow flag (register TIM1FG=1) when the content data of Timer 1 from FFH to 00H, and Timer 1 will continue counting from 00h to FFh periodical repeat automatically.

6.6. Reset

The "system resetb" signal is combine with four signals which are power on reset, low voltage reset (LVR), external RSTB pin and WDT overflow reset. A dedicated RSTB pin is provided to reset this chip by external. For normal operation of this chip, a good RSTB is needed. This pin provided built-in 150K ohm pull up resistor. The MCU will go back to NORMAL mode when RSTB was occurred in HALT mode.



6.7. Low Voltage Reset

When VDD power is applied to the chip, the low voltage RSTB default is enabled initially, it will be disabled when in halt mode. The internal system RSTB will be generated if VDD power below about V_{LVR}(1.6V)

6.8. System Clock Oscillator

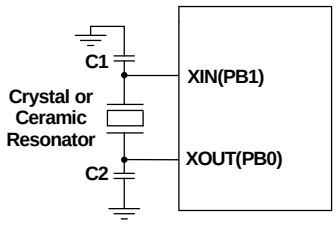
The HB8102P is provided internal high speed RC oscillator (HRCOSC) and external X'tal oscillator or ceramic resonator (XTOSC) for many application requirements. It's a dual clock MCU system.

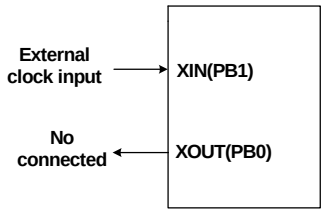
Condition VDD=2.4V~3.6V

TYPE	OSC frequency	MCU clock (F_{MCK})
HRCOSC	(1) 32MHz ±2% (2) 32MHz -15%~+15%by PB0/OSC pin	F_{HRCOSC}/8/16/32/128MCU run at 4 MHz/2MHz/1MHz/250KHz by option
XTOSC	1MHz~16MHz	F_{XTOSC}/2/4/8/16 if use 4MHz crystal MCU run at 2MHZ/1MHz/500KHz/250KHz

System clock can be stopped by HALT command. Once stopped, only wake-up triggering inputs (PA0~PA3, PB0~PB3, PD0~PD3 or PC0) or RSTB (if PA3 set as RSTB by option) can re-start oscillation. Such oscillation will do 'stable check' before release control to software. There are 128 MCU cycles stable clock delay, It's arrange after first clock output of HRCOSC/XTOSC and before user's first instruction, it means the user's program will get more stable clock after power on reset or wake up from halt mode.

XTOSC: External X'tal oscillator, XIN and XOUT are shared with PB1 and PB0 by option, suitable connected with external ceramic resonator/crystal 1MHz~16MHz. It can be driven by external clock in this mode also, no crystal or resonator needed. The picture as shown below.





6.9. I/O Port

This chip provided total 12 I/O ports, they are bi-direction I/O port PA0~PA2, PB0~PB3, PD0~PD3 and PC0, the I/O ports provided with input and output direction controlled by IOC_PA, IOC_PB, IOC_PD and IOCPC0, and all I/O also provided wake up and pull up resistor function by control register.

6.9.1. Port A /Port B (input/output)

Common I/O

Symbol	Addr	R/W	RSTB	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	USER0	IOCA2	IOCA1	IOCA0	IOCA0~IOCA2: control Port A I/O direction. 1: set PA0~PA2 as output port. 0: set PA0~PA2 as input port of corresponding PA0~PA2 bit USER0: 1 bit user RAM
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read Port A data from PA0~PA3 port and write data to PA0~PA2 (I/O direction is defined by IOC_PA register)
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	IOCB0~IOCB3: control Port B I/O direction. 1: set PB0~PB3 as output port 0: set PB0~PB3 as input port of corresponding PB0~PB3 bit
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read Port B data from PB0~PB3 port and write to PB0~PB3 (I/O direction is define by IOC_PB register)

Extended I/O

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled

The Port A and Port B are 4-bit I/O port except PA3 is an input port. They can be bit programmable setting as input port or output port. In output mode, the data can be written out to external pin by DATA_PA OR DATA_PB register, and reading this output port will get data from DATA_PA or DATA_PB register. Pull-up resistor (150K ohm) will be disabled when output mode is selected.

In input mode, Port A and Port B data can be read from external pin by reading DATA_PA or DATA_PB register, and they are provided pull-up resistor 150K or not by PAPU, PBPU registers.

In addition, each pin of Port A and Port B also can be with wake up function by using register PAWK or PBWK setting to 1. In HALT mode, If Port A or Port B with wake up enabled by these registers, any edge trigger (rising or falling) is occurred on Port A or Port B will wake up system and turn on HRCOSC or XTOSC oscillator, and the program counter of MCU will jump to the address 04H, running the wake up sub-routing program.

PA3 is an input pin only, provided with pull up 150K ohm and edge wake up function. It's shared with external reset pin (RSTB) pin by option, and VPP pin

PB0 is shared with XOUT by option and PB1 is shared with XIN pin by option. These XIN and XOUT PIN can be connected to external X'tal to replace internal oscillator HRCOSC.

6.9.2. Port C (output)

PC0 is an bi-direction I/O port and it can be set as input port or output port by IOCPC0 register.In addition, it also provided edge trigger (rising or falling) wake up function and pull up resistor.

PC1(IROUT) is an open drain output port with large sink current structure, the IR wave form generated from IR function generator and output to PC1(IROUT) pin. The IR function generator can generate different duty and frequency by IR_DIV register defined.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PC_CTRL	04H	R/W	xxxx	PC0PU	PC0WK	IOCPC0	DPC0 (R/W)	DPC0(PC0 PIN) is an bi-direction I/O port. IOCPC0: control PC0 IO direction. 1: set PC0 as output port. 0: set PC0 as input port PC0WK: wake up enable control 0: PC0 wake up disabled 1: PC0 wake up enabled PC0PU: control PC0 pull up resistor. 0: PC0 pull up resistor disabled 1: PC0 pull up resistor enabled
IR_DIV	13H	R/W	0000	DPC1 (IROUT)	IRDIV2	IRDIV1	IRDIV0	DPC1(PC1/IROUT) is an output port for IR LED driving. IRDIV2~IRDIV0: define output frequency and duty of IROUT pin

The IR_DRV register vs. PC1(IROUT) PIN definition table:

There are two type clock source selected by XTEN option when use IR LED function generator.

1.If XTEN=0, Internal RC OSC enabled, IR clock source (F_{IR}) = 32MHz/8= 4MHz

2.If XTEN=1, External X'tal OSC enabled, IR clock source (F_{IR}) = external X'tal frequency = 4MHz

(Notice : PB0 and PB1 pin must be connected to 4MHz crystal in this mode)

IRDIV2~IRDIV0 registers	Internal Divider	IROUT PIN output duty & frequency	
		Duty	Frequency
000	x	x	DPC1 register output to IROUT pin
001	F_{IR} /105	52/105 (1/2)	38.09KHz
010	F_{IR} /105	1/3	38.09KHz
011	F_{IR} /70	1/2	57.14KHz
100	F_{IR} /71	23/71 (1/3)	56.33KHz
101	F_{IR} /95	31/95 (1/3)	42.10KHz
110	F_{IR} /100	33/100 (1/3)	40.00KHz
111	F_{IR} /111	1/3	36.03KHz

6.9.3 Port D (input/output)

Reserved	0BH	R/W	xxxx	X	X	X	X	Reserved
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	IOCD0~IOCD3: control Port D I/O direction. 1: set PD0~PD3 as output port. 0: set PD0~PD3 as input port of corresponding PD0~PD3 bit
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read Port D data from PD0~PD3 port and write to PD0~PD3 (I/O direction is define by IOC_PD register)
PDPU	04H	W	0000	PDPU.3	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
PDWK	08H	W	0000	PDWK.3	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled

Whether all 4 bits of the Port D is input or output port depends on IOC_PD control register.

Port D also provided edge trigger (rising or falling) wake up and pull up resistor 150K, function just like Port A or Port B.

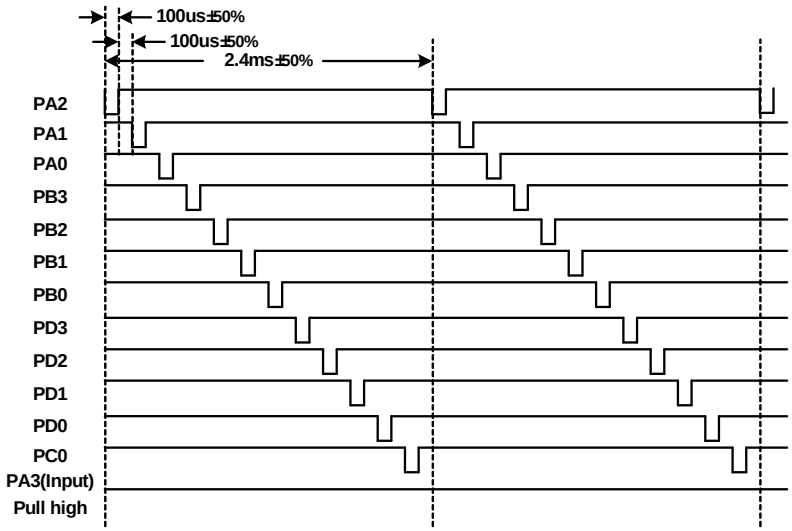
5.9.4. Wake up function for keyboard scan in halt mode

All Port A, Port B, PC0, Port D are provided a special wake up function for hardware keyboard scan in halt mode automatically, and this function can be enabled by code option and enabled or disabled for individual PIN by corresponding wake up registers.

It's built-in one low power RC oscillator 20KHz ± 50% for the clock of keyboard scan function operation.

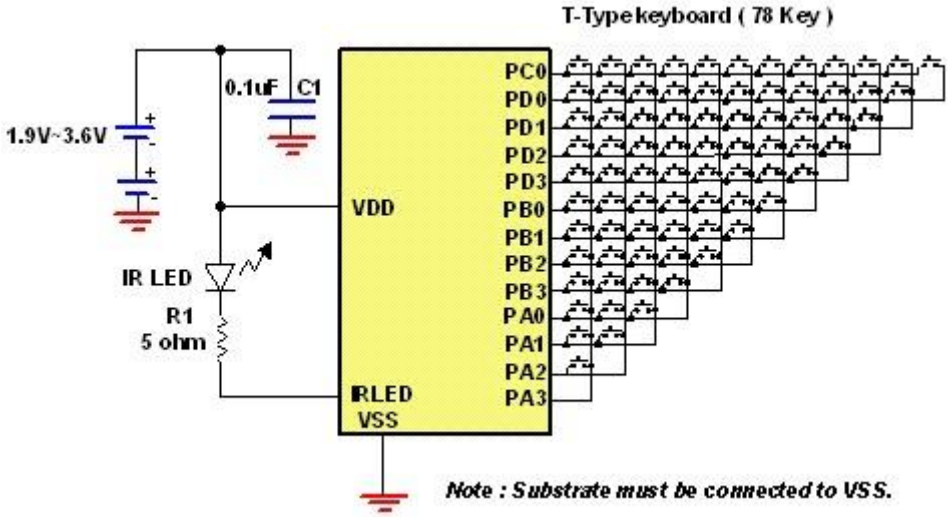
The detail action of keyboard scan is described below:

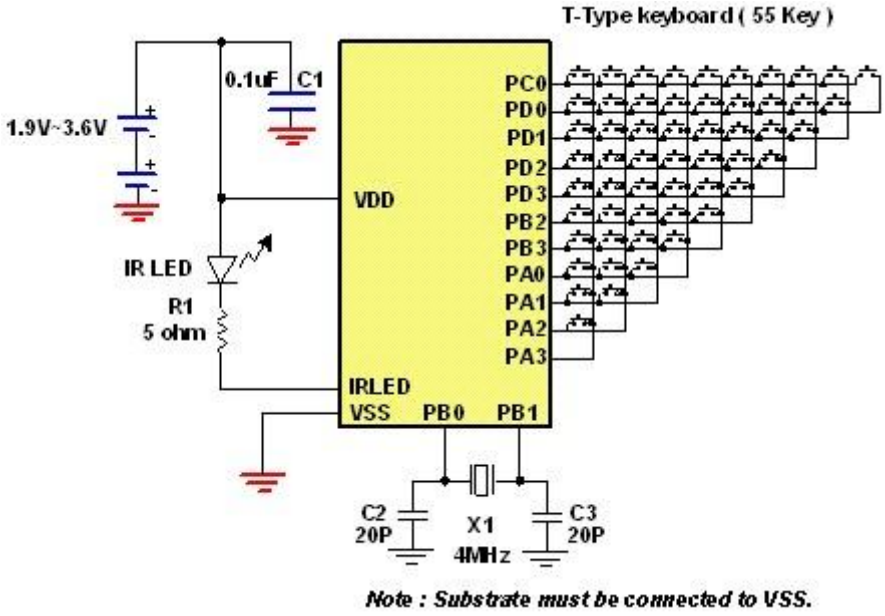
1. Keyboard scan function enabled by code option KBSCEN.
2. Set all scan key I/O to input mode.
3. Pull up resistor enabled by PAPU, PBPU, PC0PU, PDPU register.
4. Wake up function enabled by PAWK, PBWK, PC0WK, PDWK register. Keyboard scan function can be
   disabled for individual pin by corresponding wake up control registers set to 0.
5. Execute HALT instruction into power down mode.
6. When in halt mode, only one I/O port direction switch to output state and others are in input state with pull up resistor. The output port will output one low-pulse from PA2~PA0, PB3~PB0, PD3~PD0 and PC0 sequentially if all wake up registers of all I/O port is enabled. The period of keyboard scan time is fixed (about 2.4ms ± 50%), even only 1 port enabled keyboard scan function. The I/O direction won't be changed if the keyboard scan function of specified I/O port disabled by wake up registers (PAWK, PBWK, PC0WK or PDWK register).
7. In halt mode, MCU will be waked up by rising or falling edge of I/O ports which key scan function is enabled.



The waveform of keyboard scan function

7、Application Circuit





8、Internal Option Registers

<table>
<tr><th>Option Name</th><th>Function Description</th></tr>
<tr><td>WDTEN</td><td>WDT enable/disable control
0: WDT enabled (WDT period is 1 second)
1: WDT disabled</td></tr>
<tr><td>PA3_RSTB</td><td>PA3 pin shared with RSTB pin control
0: PA3 is RSTB pin
1: PA3 is normal I/O port</td></tr>
<tr><td>XTENB</td><td>External crystal mode enabled/disabled
0: External crystal mode enabled, PB0, PB1 should be connected to External X’tal.
1: External crystal mode disabled, PB0, PB1 is I/O port function.</td></tr>
<tr><td>MCKS1
MCKS0</td><td>MCU operating clock define (external crystal frequency= F_{XTAL})
<table>
<tr><th>MCKS1</th><th>MCKS0</th><th>Option XTENB=1
Use internal HRCOSC</th><th>Option XTENB=0
Use external EXTOSC (F_{XTAL})</th></tr>
<tr><td>0</td><td>0</td><td>MCU run at 250KHz</td><td>MCU run at F_{XTOSC} /16</td></tr>
<tr><td>0</td><td>1</td><td>MCU run at 1MHz</td><td>MCU run at F_{XTOSC} /8</td></tr>
<tr><td>1</td><td>0</td><td>MCU run at 2MHz</td><td>MCU run at F_{XTOSC} /4</td></tr>
<tr><td>1</td><td>1</td><td>MCU run at 4MHz</td><td>MCU run at F_{XTOSC} /2</td></tr>
</table></td></tr>
<tr><td>KBSCEN</td><td>keyboard scan option enabled/disabled
0: Keyboard scan function disabled
1: Keyboard scan function enabled</td></tr>
</table>

9、Revision History

Version	Description	Page	Date
V1.0.0	Established		Mar. 1, 2011
V1.0.1	1. LVR=1.5V 2. Added Package SOP8 3. Delete “except indirect operation is used”	P1 P2 P5	Apr, 6 2011
V1.0.2	1. Sink current : I_{OL}=210mA at VDD=3V and V_{OL}=0.3V requency deviation within ±2%, VDD=1.8V~3.6V,temp= -20 ºC ~70 ºC 2. It’s provided only one time-out period 1sec	P1 P8	Apr,21 2011