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浩博高科技

HB8101Pk Remote controller

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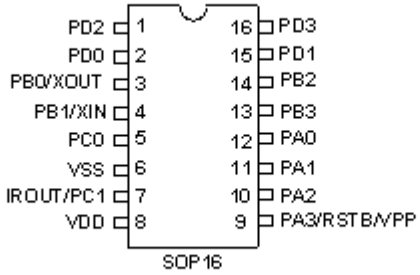
1. General Descriptions

The HB8101Pk series are a high-performance 4-bit RISC micro-controller embedded with 640X12 bits OTP, 32X4 bits SRAM, 12 Input/Output pins, one input pin, T-type keyboard scan and built-in one IR LED driver pin. it's flexible and cost-effective solution for remote control of TV, Fans, Air conditioners ... etc.

2. Features

- MCU Operating voltage: 1.8V to 3.6V
- MCU run 2 MIPS
- Memory Size
  Program ROM size : 640 X12 bits (OTP type)
  SRAM size : 32x4 bits
- Wake up function for power-down mode
  HALT mode wake up source : PA0~PA3, PB0~PB3, PD0~PD3 and PC0 edge trigger.
- 12 input /output ports : PA0~PA2, PB0~PB3, PD0~PD3 and PC0. Each I/O can be bit programmable as input or output port. These 12 I/Os also provided level-change-wakeup function. Pull up resistor setting is available by software.
  (a) They are provided with high sink current 20mA @VDD=3V, V_{OL}=0.5V.
  (b) They are provided with drive current 7mA @VDD=3V, V_{OH}=2.5V.
  (c) Pull up 150k ohm resistor.
- Built-in one IR LED driver pin. (Sink current : I_{OL}=210mA @VDD=3V and V_{OL}=0.3V)
- T-type keyboard scan.
- One 8 bits timer, clock source of timer comes from F_{MCK} divided by 8192 (or 4096,2048,1024), the content of timer can be cleared and read by program.
- Built-in internal RC OSC 8 MHz ----
  frequency deviation within ± 2 %, VDD=1.8V~3.6V, temp= - 20 ºC ~ 70 ºC
- Three reset condition
  - □ Low voltage reset (LVR=1.5V)
  - □ Power on RC-reset
  - □ Watch dog timer overflow reset (WDT period is 0.262 Sec)

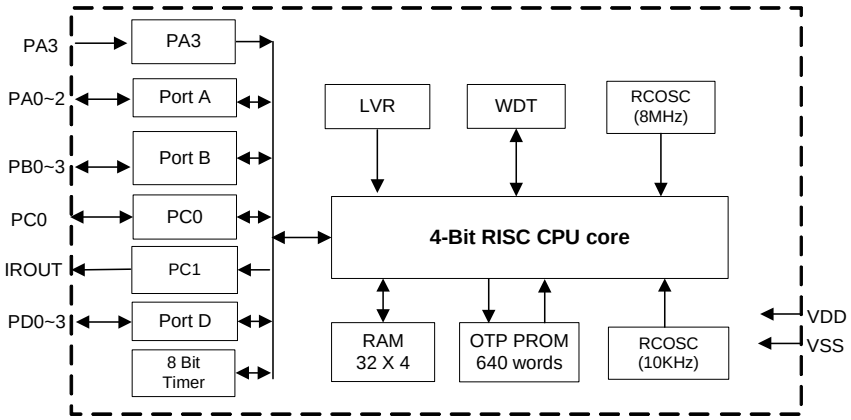
Package SOP16



3. Pads Information

PAD Name	Type	State After Reset	Description
Reset/Power Input			
VDD	I	High	Power input pin.
VSS	I	Low	Ground input pin.
General I/O ports			
PA0~PA2	I/O	XXXX	PA0~PA2 are programmable I/O pin with pull up resistor 150k ohm. Level-change-wakeup function is provided.
PA3/VPP	I	X	PA3 is an input pin only, with pull up resistor 150K ohm. Level-change-wakeup function is provided.
PB0~PB3	I/O	XXXX	PB0~PB3 are programmable I/O pin with pull up resistor 150k ohm. Level-change-wakeup function is provided.
PC0	I/O	X	PC0 is programmable I/O pin with pull up resistor 150k ohm. Level-change-wakeup function is provided.
IROUT	O	X	IROUT is an IR signal output pin. Open drain and high sink current type.
PD0~PD3	I/O	XXXX	PD0~PD3 are programmable I/O pin with pull up resistor 150k ohm. Level-change-wakeup function is provided.

Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-20 to 70	ºC

Storage Temperature	T_{STO}	-50 to 150	ºC

4.2 DC/AC Characteristics

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{DD}	-	1.8	-	3.6	V
Operating Current	I_{OP1}	VDD=3V , MCU run 2 MIPS	-	0.45	-	mA
Standby Current 1	I_{STBY1}	MCU stop, WDT off,	-	0.1		uA
Standby Current 2	I_{STBY2}	MCU stop All I/O port no loading Key Scan option on	-	1.2		uA
Input High Level	V_{IH}	All I/O port		0.7*V_{DD}	-	V
Input Low Level	V_{IL}	All I/O port	-	0.4*V_{DD}		V
Output Drive Current	I_{OH}	VDD=3V , V_{OH}=2.5V All I/O port, except IROUT	-	-7	-	mA
Output Sink Current	I_{OL1}	VDD=3V , V_{OL}=0.5V All I/O port, , except IROUT	-	20	-	mA
IROUT PIN Output Sink Current	I_{OL2}	VDD=3V , V_{OL}=0.3V	-	210	-	mA
Input Resistor	R_{up}	Pull up 150K ohm	135	150	165	K ohm
LVR	V_{LVR}			1.5		V
SRAM Data Retention voltage	V_{DR}		1.4			V

AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Internal HRCOSC Frequency	F_{OSC1}	VDD = 1.8V~3.6V Temp.= -20 ºC ~ 70 ºC	7.904	8 ± 1.2%	8.096	MHz
MCU Operation frequency	F_{MCK}	VDD=1.8V~3.6V		2 ± 1.2%		MIPS
MCU Operation voltage	V_{OP}		1.8	3.0	3.6	V
Internal LRCOSC Frequency	F_{LOSC}	VDD=3V		10KHz ± 50%		KHz
WDT period	T_{WDT}	VDD=1.8V~3.6V		(2^20)/F_{MCK} =0.262		Sec
Stable clock delay after power on or system reset	CKstable1	(Note 1)	-	2318 x (1/ F_{MCK})		us
Stable clock delay after wake up	CKstable2	System oscillator --HRCOSC (Note 2)	-	64 x (1/ F_{MCK})		us

Note1: The stable clock delay (CKstable1) is a delay between HRCOSC-started and 1st instruction-execution. This delay will ensure stable system clock after power on or reset.

Note2: The stable clock delay (CKstable2) is a delay between HRCOSC-started and 1st instruction-execution of wakeup. This delay will ensure stable system clock after wake up.

Note3: F_{MCK} is MCU operating clock.

5. Functional Description

This MCU inside HB8101Pk is a high performance process. The operation speed is fixed on 2 MIPS.

5.1 Program ROM (PROM)

HB8101Pk supports 640 words OTP PROM which is located on $000h ~ $25Fh and $260h ~ $27Fh, the first area $000h ~ $25Fh stores user program area, and the second area $260h ~ $27Fh named reserved area, they can't read by program. The OTP PROM memory plan is shown below:

Address	HB8101Pk (0.6 K OTP PROM)
000h ~ 0FFh	User area 606 words
100h ~ 1FFh	
200h ~ 25Dh	
25Eh ~ 25Fh	Serial number area (2 words)
260h ~ 27Fh	Reserved area

Note: 1. For HB8101Pk, the content of OTP PROM address $000h~$25Fh can be read by program. Address $260h~$27Fh can't be read by program.

2. If DMA2~DMA0 pointed address is located at invalid address 260h~27Fh , the register DMA2.1 will be changed to 0 by hardware automatically, the register DMA2.0, DMA0 and DMA1 will not be affected.

3. To read DMDL, DMDM and DMDH registers, only LD A,(n) instruction can be used. Other instructions are not allowed. (n= DMDL, DMDM or DMDH)

To read OTP PROM data, use DMA2~DMA0 registers as address pointer. The address range is located in $000h ~ $25Fh. After these registers (DMA0~2) are specified by software, the 12bits data of ROM can be moved to A register by three instructions, they are "LD A, (DMDL)", "LD A, (DMDM)" and "LD A, (DMDH)". The three instructions mentioned above are two cycle instruction, all others instructions are single cycle instruction.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2 build a 10 bit addressing space for read ROM data. DMA0 is the lowest nibble address, DMA2 is the highest nibble address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	00xx	**0**	**0**	DMA2.1	DMA2.0	
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data from PROM that addressed by DMA0 ~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	(1) DMDM is used to read middle nibble data from PROM that addressed by DMA0 ~ DMA2. (2) Write this register with data 05h will clear watch dog timer (WDT)
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read high nibble data from PROM that addressed by DMA0 ~ DMA2.

For example, assume the data of address 156H is 587H.

```
LD A, #1
LD (DMA2), A
LD A, #5
```

```
LD (DMA1), A
LD A, #6
LD (DMA0), A       ; PROM address = 156H
LD A, (DMDL)       ; A register = 7H; low nibble data of PROM address 156H
LD A, (DMDM)       ; A register = 8H; middle nibble data of PROM address 156H
LD A, (DMDH)       ; A register = 5H; high nibble data of PROM address 156H
            .......
```

5.2 SRAM and I/O Memory Map

HB8101Pk provides 32 nibbles SRAM on the locations $20H~$3FH. This addressing space of SRAM is different from PROM's address.

Direct Addressing (use MAH)		Real SRAM Address	SRAM MAP
MAH=XH (MAH no effect)	00H~1FH		Common I/O port and SFR(special function register) register
MAH=0H	20H~3FH	00H~1FH	USER SRAM (32x4)

5.2.1 I/O Memory Map

The I/O memory map consists of common I/O, control registers and extended I/O space. Detailed operations are as follows.

5.2.2 Common I/O

The "common IO block" contains 32 addresses. All registers in this block can be accessed directly by these instructions : LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR. SET, CLR (bit set/clear) can only operate on the address range from 00H to 0FH.
Read common I/O instruction: LD/ADC/SBC/CMP/OR/AND/XOR (Ex. LD A,(n))
Write data to common I/O instruction: LD (n),A
Read and write common I/O instruction : DEC/INC/ADR/RRC/RLC (Ex. DEC (n))

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	0	0	CF	ZF	ZF : Zero status register CF : Carry status register
Reserved	01H	R/W	xxxx	X	X	X	X	Reserved
IOC_PA	02H	R/W	0000	USER0	IOCA2	IOCA1	IOCA0	Port PA0~PA2 input/output direction : 1: set port as output port individually 0: set port as input port individually USER0: 1 bit user register.
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read data from PA0~PA3 PIN and write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
PC0_CTRL	04H	R/W	000x	PC0PU	PC0WK	IOCPC0	DPC0 (R/W)	DPC0 (PC0 PIN) is an bi-direction I/O port. IOCPC0: control PC0 IO direction. 1: set PC0 as output port. 0: set PC0 as input port

								PC0WK: wake up enable control 0: PC0 wake up disabled 1: PC0 wake up enabled PC0PU: control PC0 pull up resistor. 0: PC0 pull up resistor disabled 1: PC0 pull up resistor enabled
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	Port PB0~PB3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register)
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user RAM
Reserved	08H~ 0BH	R/W	xxxx	X	X	X	X	Reserved
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	Port PD0~PD3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read data from PB0~PB3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register)
SCALER1	0EH	R/W	0000	TM1EN	TM1FG	T1DIV1	T1DIV0	T1DIV1~T1DIV0: The pre-scaler of TIMER1 Timer 1 clock source definition table F_{MCK} = MCU operating clock T1DIV1 | T1DIV0 | TM1CK 0 | 0 | F_{MCK}/8192 0 | 1 | F_{MCK} /4096 1 | 0 | F_{MCK} /2048 1 | 1 | F_{MCK} /1024 TM1FG: Timer 1 overflow flag 0: no overflow occurred. 1: overflow occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user RAM
TIM1_L	11H	R	0000	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0000	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
IR_DIV	13H	R/W	1000	DPC1 (IROUT)	IRDIV2	IRDIV1	IRDIV0	DPC1 is an output register for IROUT PIN. IRDIV2~IRDIV0: duty and frequency selection.
Reserved	14H~ 17H							Reserved
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2 build a 10 bit addressing space for read PROM data. DMA0 is the lowest nibble address, DMA2 is the highest nibble address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	**00xx**	**0**	**0**	DMA2.1	DMA2.0	
Reserved	1BH	x	xxxx	x	x	x	x	Reserved
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data from PROM that addressed by DMA0 ~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	(3) DMDM is used to read middle nibble data from PROM that addressed by DMA0 ~ DMA2. (4) Write this register with data 05h will clear watch dog timer (WDT)

DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read high nibble data from PROM that addressed by DMA0 ~ DMA2.
Reserved	1FH	R/W	xxxx	X	X	X	X	Reserved
SRAM 32 nibbles	20H~ 3FH	R/W	xxxx	SRAM.3	SRAM.2	SRAM.1	SRAM.0	SRAM

5.2.3 Extended I/O

To extend I/O memory space, HB8101Pk provided one special instructions, “LD **EXIO**(n), A”, where n = 00H ~ 0FH” to obtain the 16 extra I/O registers. These registers are used for the I/O port pull up resistors control and wake up control, they can be accessed by two “LD” data transfer instruction only.
For example, the pull up resistor of Port A is enabled, the program as shown below:

```
LD A, #FH
LD EXIO(00H), A
```

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
Reserved	01H	X	xxxx	X	X	X	X	Reserved
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
Reserved	03H	X	xxxx	X	X	X	X	Reserved
PDPU	04H	W	0000	PDPU.3	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
Reserved	05H	X	xxxx	X	X	X	X	Reserved
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled
PDWK	08H	W	0000	PDWK.3	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled
Reserved	09H~ 0FH							Reserved

5.3 Halt Mode & Wake up

The MCU operation may be switched to HALT mode (HRCOSC stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3 , PD0~PD3 and PC0 are provided with wake up function on rising edge or falling edge. When wake up condition occurred, program will start from $004H address after stable clock delay (CKstable1). “system reset” signal will release HALT state and execute reset procedure. SRAM will keep their previous data without change in HALT mode.

5.4 Watch Dog Timer Reset (WDT)

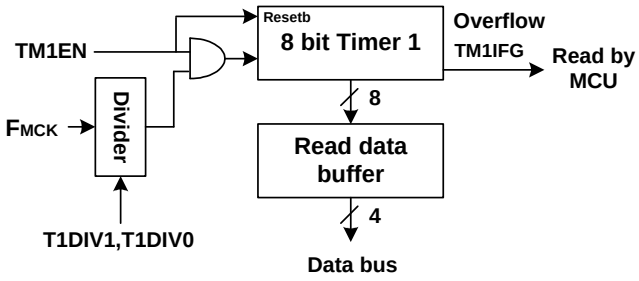
The watch dog timer (WDT) is used to reset chip when unexpected execution sequence caused, avoiding dead lock of MCU program. This timer can be enabled or disabled by option only. WDT will not have any action when WDT option disabled. Software shall run an "clear watch dog timer" (write data 05h to register $1D) instruction before WDT time out if WDT option is enabled. Hardware will generate a reset signal to reset whole system when WDT overflow. It's provided with only one time-out period (0.262 sec.). The clock source of WDT comes from MCU clock.

WDT will be reset when wake up from HALT mode, power on reset or cleared by software. The watch dog timer can be reset by following program :

```
LD      A, #05H
LD  (1DH), A    ; clear watch dog timer
```

Notice: For good system reliability, It's strongly recommended that, do not use more than one "reset watch dog" instruction in whole program.

5.5 Programable 8 bits TIMER1



The Timer 1 is an 8 bit up timer. The overflow interval can be easy generated by reading the content value of timer 1, and Timer 1 can be cleared to 00h by setting TIM1EN=0. The content value of Timer 1 can be readable by program.
The interrupt isn't provided in HB8101Pk, using polling TM1FG is only the way to check out overflow.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
TIM1_L	11H	R	0000	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0000	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.

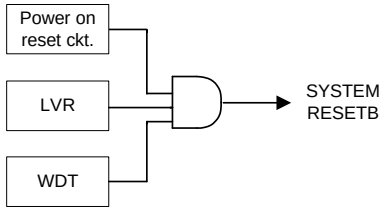
SCALER1	0EH	R/W	0000	TM1EN	TM1FG	T1DIV1	T1DIV0	T1DIV1~T1DIV0: The pre-scaler of TIMER1 Timer 1 clock source definition table F_{MCK} = MCU operating clock T1DIV1 / T1DIV0 / TM1CK 0 / 0 / F_{MCK}/8192 0 / 1 / F_{MCK} /4096 1 / 0 / F_{MCK} /2048 1 / 1 / F_{MCK} /1024 TM1FG: Timer 1 overflow flag 0: no overflow occurred. 1: overflow occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled

The clock source of Timer 1 can come from the frequency divider, there are 4 kinds of clock rate selected by register T1DIV1 and T1DIV0 in this divider, and the divider's clock source is come from MCU operation clock.
TM1CK= Timer 1 clock source (**F_{MCK}** = MCU operating clock)

T1DIV1	T1DIV0	TM1CK
0	0	**F_{MCK} /8192**
0	1	**F_{MCK} /4096**
1	0	**F_{MCK} /2048**
1	1	**F_{MCK} /1024**

The 8 bits content of Timer 1 can be reset to 00h by TMI1EN setting to 0, it will be up count while Timer 1 clock source is rising after TIM1EN setting to 1. The read operation sequence of TIM1.7~TIM1.0 must be follow low nibble (TIM1_L) first and high nibble (TIM1_H) later. The Timer 1 will issue an overflow flag (register TM1FG=1) when the content data of Timer 1 from FEh to FFh occurred, and Timer 1 will continue counting from FFh, 00h, 01h… to FFh periodical repeat automatically.

5.6 Reset



The actual system reset of this chip combines with three signals, which are power on reset, low voltage reset (LVR) and WDT overflow reset. MCU will go to NORMAL mode when system reset occurred.

5.7 Low Voltage Reset

When VDD power is applied to the chip, the low voltage reset circuit is enabled initially, it will be disabled when in HALT mode. The internal system reset will be generated if VDD is lower than V_{LVR}.

5.8 System Clock Oscillator

The HB8101Pk is provided an internal high speed RC oscillator (HRCOSC), this HRCOSC provided a precision frequency deviation under ± 1.2% at VDD from 1.8V to 3.6V and temperature from -20℃ to +70℃.

Condition VDD=1.8V~3.6V

TYPE	OSC frequency	MCU clock (F_{MCK})
HRCOSC	8MHz ± 1.2%	F_{HRCOSC} /4 , MCU run 2 MIPS

System clock can be stopped by HALT command. Once stopped, only wake-up triggering inputs (PA0~PA3, PB0~3, PD0~PD3 or PC0) can release HALT mode and re-start oscillator. Such oscillator will do 'stable check' before release control to software. In order to make system stable, the stable clock delay *(CKstable2)* must be placed between oscillator starting and first instruction of user software. Refer to table on page 4.

5.9 I/O Port

HB8101Pk provides totally 12 I/O ports and one input port. There are four bi-direction I/O ports, Port A ,Port B, Port D and PC0. Input and output direction is controlled by IOC_PA, IOC_PB, IOC_PD and IOCPC0. PA3 are input pin only. All I/O are provided with wake up and pull up resistor function by control registers.

5.9.1 Port A /Port B (input/output)

The Port A and Port B are 4-bit I/O port. Each bit (pin) can be individually set as input port or output port except PA3. In output mode, data can be written to external pin. In output mode, reading I/O port will read internal register data not external pin. Built-in pull-up resistor will be disabled when in output mode.
In input mode, Port A and Port B data are read voltage from external pin. These pins can have pull-up resistor 150K or not. They are selected by PAPU or PBPU registers.
Each pin of Port A and Port B can be selected with wake up function or not by register PAWK or PBWK. In HALT mode, If Port A or Port B wake-up function is enabled. Any rising or falling signal on these selected ports will wake up system and turn on HRCOSC simultaneously. Program counter of MCU will jump to address 04H to run wake up program.
When Port A and Port B are selected as wake-up enabled, and system enters HALT by HALT instruction. Then, these ports will enter input mode automatically even if they are set as output ports previously. This function is not provided for PA3.

Common I/O

Symbol	Addr	R/W	RSTB	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	USER0	IOCA2	IOCA1	IOCA0	Port PA0~PA2 input/output direction : 1: set port as output port individually 0: set port as input port individually USER0: 1 bit user register.
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read data from PA0~PA3 PIN and write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	Port PB0~PB3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register)

Extended I/O

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled

PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled

5.9.2 Port C (Output)

PC0 is a bi-direction I/O port and it can be set as input port or output port by IOCPC0 register. In addition, it is also provided edge trigger (rising or falling) wake up function and pull up resistor.
PC1(IROUT) is an open drain output port with large sink current structure, it can output the IR waveform from IR function generator . The duty and frequency of IR function generator is selectable by IR_DIV2~ IR_DIV0 registers.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PC_CTRL	04H	R/W	xxxx	PC0PU	PC0WK	IOCPC0	DPC0 (R/W)	DPC0(PC0 PIN) is an bi-direction I/O port. IOCPC0: control PC0 IO direction. 1: set PC0 as output port. 0: set PC0 as input port PC0WK: wake up enable control 0: PC0 wake up disabled 1: PC0 wake up enabled PC0PU: control PC0 pull up resistor. 0: PC0 pull up resistor disabled 1: PC0 pull up resistor enabled
IR_DIV	13H	R/W	1000	DPC1 (IROUT)	IRDIV2	IRDIV1	IRDIV0	DPC1 is an output register for IROUT PIN. IRDIV2~IRDIV0: duty and frequency selection.

The IR_DRV register vs. PC1(IROUT) PIN definition table:
The clock source of IR function generator is named F_{IR}, F_{IR} = F_{HRCOSC} = 8MHz.

IRDIV2~IRDIV0 registers	IR function generator	Internal Divider	IROUT PIN output duty & frequency	
			Duty	Frequency
000	disabled	x	IROUT pin is controlled by DPC1 register Low period/Total period	
001	enabled	F_{IR} /222	74/222 (1/3)	36.04KHz
010	enabled	F_{IR} /218	73/218(1/3)	36.70KHz
011	enabled	F_{IR} /211	70/211(1/3)	37.91KHz
100	enabled	F_{IR} /211	106/211(1/2)	37.91KHz
101	enabled	F_{IR} /211	141/211(2/3)	37.91KHz
110	enabled	F_{IR} /200	67/200(1/3)	40.00KHz
111	enabled	F_{IR} /142	47/142(1/3)	56.34KHz

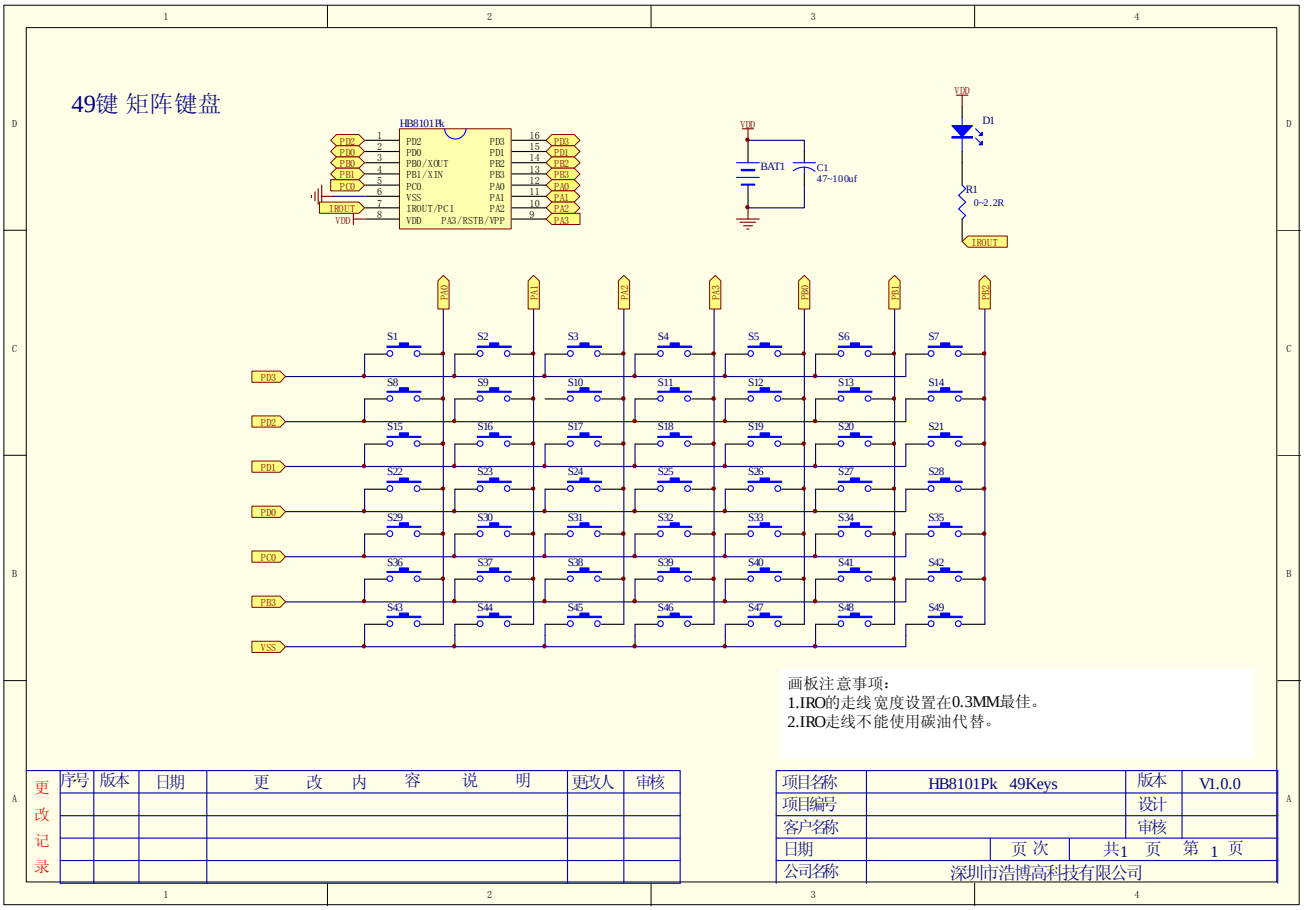
5.9.3 Port D (input/output)

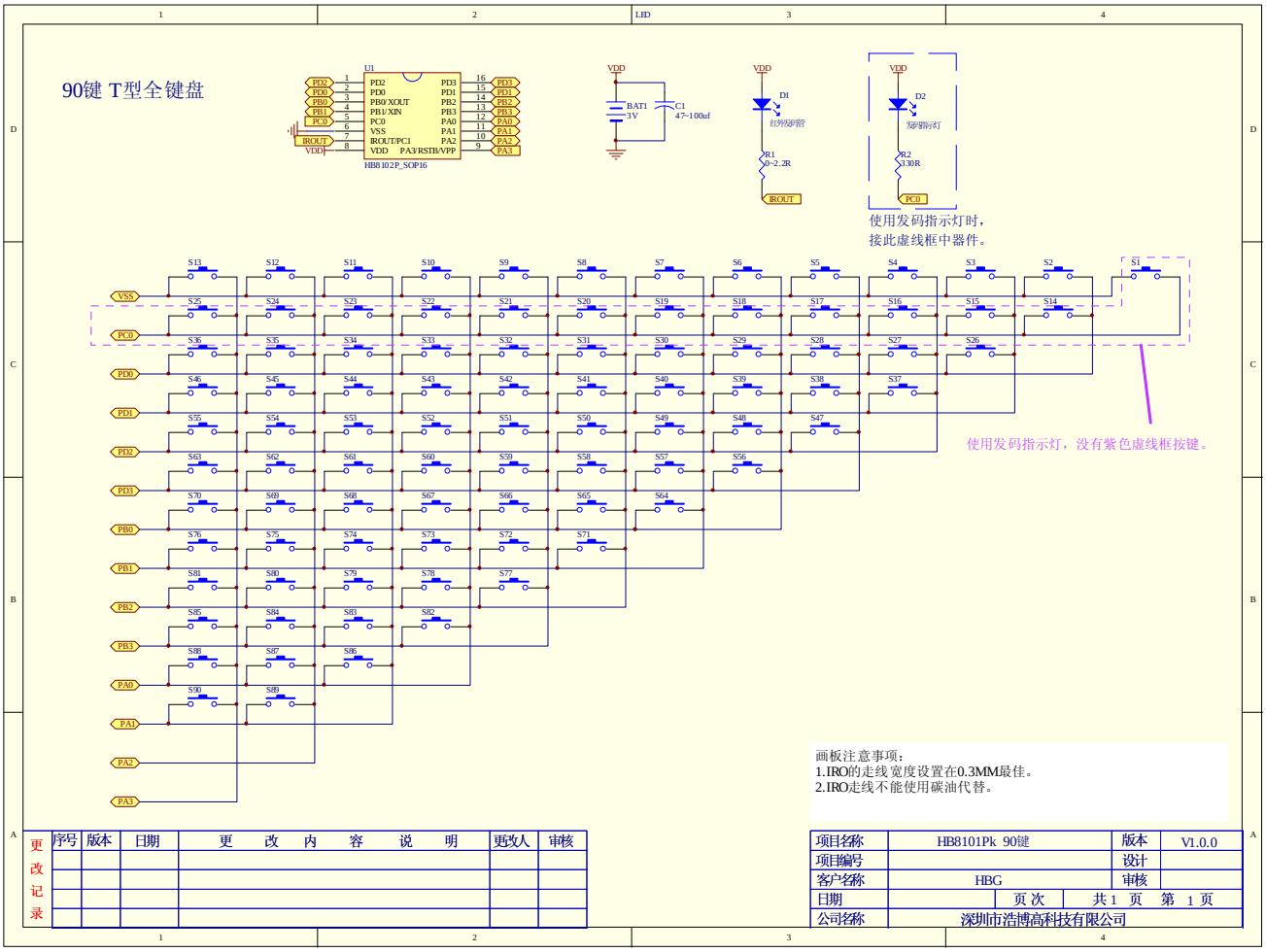
Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	Port PD0~PD3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read data from PB0~PB3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register)

PDPU	04H	W	0000	PDPU.3	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
PDWK	08H	W	0000	PDWK.3	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled

IOC_PD register defines the input/output selection of PD0~PD3.
PDWK register defines wake up function of PD0~PD3.
PDPU defines the existence of 150K pull up resistor in input mode, just like Port A or Port B.

6. Application Circuit





7. Internal Option Registers

Option Name	Function Description
SECURITY	OTP data readable/unreadable.
KBSCEN	key option enabled/disabled control

8. Revision History

Version	Description	Page	Date
V1.0.0	Established		Jan. 7. 2013
V1.0.1	Updata Reference Circuit		Jan. 23. 2013