General Description

The LSP5311 is a high efficiency monolithic synchronous buck regulator using a constant frequency, cur-rent mode architecture. Capable of delivering 1A output current over a wide input voltage range from 2.7V to 5.5V.

Supply current with no load is 400μA and drops to<1μA in shutdown. The 2.7V to 5.5V input Voltage range makes the LSP5311 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low drop-out operation, extending battery life in portable systems. PWM pulse skipping mode operation provides very low output ripple voltage for noise sensitive applications. At very light load, the LSP5311 will automatically skip pulses in pulse skip mode operation to maintain output regulation.

The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.6V feedback reference voltage. The LSP5311 is available in SOT-25 packages.

Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

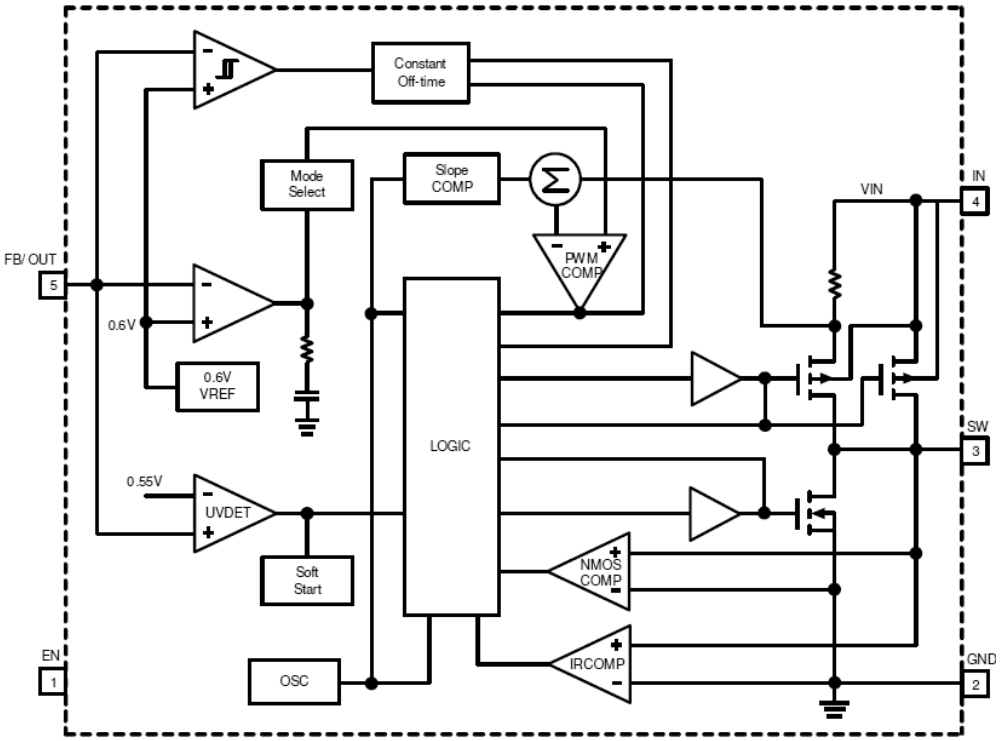
Features

- High Efficiency: Up to 95%
- Shutdown Mode Draws < 1μA Supply Current
- 2.7V to 5.5V Input Range
- Adjustable Output From 0.6V to VIN
- Adjustable Output Voltage
- 1A Output Current
- Low Dropout Operation: 100% Duty Cycle
- No Schottky Diode Required
- 1.5MHz Constant Frequency PWM Operation
- SOT-25 Packages
- RoHS Compliant and Halogen Free

Applications

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

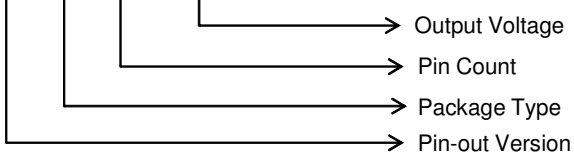
Block Diagram



Please be aware that an **Important Notice** concerning availability, disclaimers, and use in critical applications of LSC products is at the end of this document.

Ordering Information

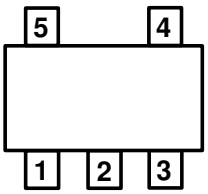
LSP 5311 X XX X XXX



Pin-out Version	Package Type	Pin Count	Output Voltage
A (SOT23-5L) 1. EN 2. GND 3. SW 4. IN 5. FB	AA : SOT23	D : 5	ADJ : Adjustable

Pin Assignment

SOT23-5L
Top View



LSP5311AAAD
01. EN
02. GND
03. SW
04. IN
05. FB

Pin Descriptions

Pin Name	Pin Description
EN	No connection. Not internally connected. Can left floating or connected to GND.
GND	Ground. Tie directly to ground plane.
SW	Switch Node Connection to Inductor.
IN	Input Supply Voltage Pin. Bypass this pin with a capacitor as close to the device as possible.
FB	Output voltage Feedback input.
OUT	Output Voltage for fixed version

Absolute Maximum Ratings (at T_A=25℃)

Characteristics		Symbol	Rating	Unit
Input Supply Voltage		VIN	6	V
EN, VOUT Voltage		VEN, VOUT	–0.3V to 6	V
SW Voltage		VSW	6	V
Junction Temperature		T_J	150	℃
Storage Temperature		T_{STG}	-60~150	℃
Power Dissipation (Note2)	SOT23-5	PD	TBD	W
Moisture Sensitivity		MSL	Please refer the MSL label on the IC package bag/carton for detail	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at TA = 25℃ on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3. The device is not guaranteed to function outside its operating conditions.

Recommended Operating Conditions

Characteristics	Symbol	Min	Max	Unit
Supply Input Voltage	VIN	2.7	5.5	V
Junction Temperature Range	T_J	-40	125	℃
Ambient Temperature Range	T_A	-40	85	℃

Electrical Characteristics

(V_{IN}=3.6V, V_{OUT}=2.5V, V_{FB}=0.6V, L=2.2µH, C_{IN}=4.7µF, C_{OUT}=10µF, T_A=25°C, I_{MAX}=1A unless otherwise specified.)

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{IN}		2.7		5.5	V
Feedback Voltage	V_{FB}	For Adjustable Output Voltage	0.588	0.6	0.612	V
Feedback Pin Bias Current	I_{FB}	V_{FB} = 0.6V	-50		50	nA
Quiescent Current	IQ	V_{FB} > 0.6V		65	80	µA
Shutdown Current	I_{SHDN}	V_{EN} = GND		0.1	1	m A
Switch Frequency	f_{OSC}		1.2	1.5	1.8	MHz
High-side Switch On-Resistance	$R_{DS,ON, LHI}$	I_{SW} = 200mA, V_{IN}= 3.6V		280		mΩ
Low-side Switch On-Resistance	$R_{DS,ON, LO}$	I_{SW}=200mA, V_{IN}=3.6V		250		mΩ
Switch Current Limit	$I_{SW,CL}$	V_{IN}=2.5 to 5.5V	1.0	1.5		A
EN High (Enabled the Device)	$V_{EN,HI}$	V_{IN}=2.5 to 5.5V	1.5			V
EN Low (Shutdown the Device)	$V_{EN,LO}$	VIN=2.5 to 5.5V			0.4	V
Input Under-voltage Lockout	V_{UVLO}	Rising edge		2.5		V
Input Under-voltage Lockout Hysteresis	$V_{UVLO,HYST}$			0.1		V
Input Voltage over shutdown	IOVP			6		V
Input over Voltage Hysteresis	IOHYS			0.1		V
Soft Start Time				1		mS

Electrical Characteristics (Contd.)

(V_{IN}=3.6V, V_{OUT}=2.5V, V_{FB}=0.6V, L=2.2µH, C_{IN}=4.7µF, C_{OUT}=10µF, T_A=25°C, I_{MAX}=1A unless otherwise specified.)

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Thermal Shutdown Temperature	OTP	Shutdown, temperature increasing		160		°C
Temperature Shutdown Hysteresis	$OTP_{(HYS)}$	Shutdown, temperature increasing		20		°C
Maximum Duty Cycle	D_{MAX}		100			%
SW Leakage Current		EN=0V, VIN=5.0V VSW=0V or 5.0V	-1		1	m A

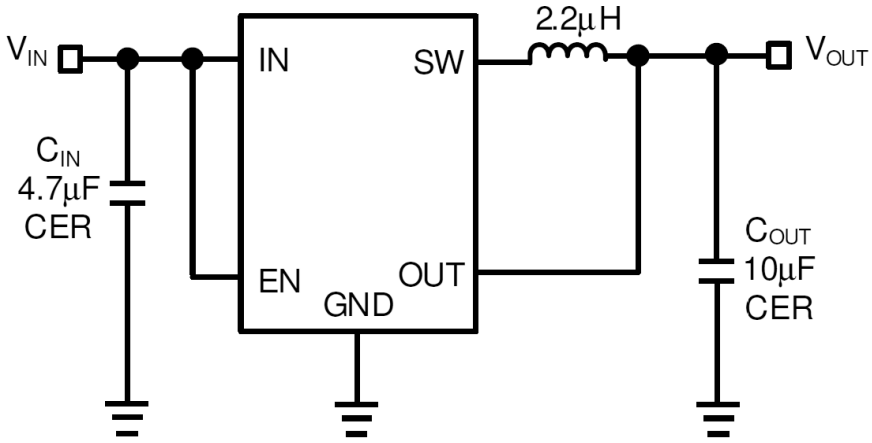
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. θJA is measured in the natural convection at TA = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Application Circuit



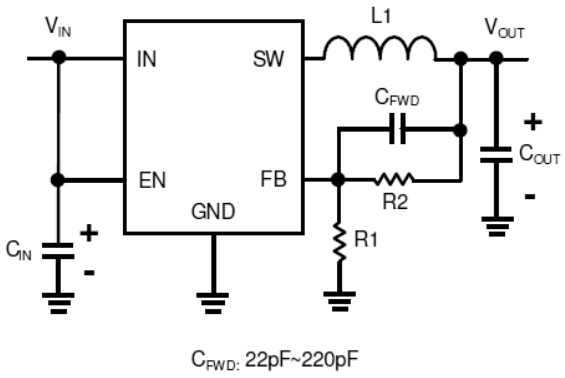
Fixed Output Voltage

Figure 1: High Efficiency Step-Down Converter

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LSP5311. These items are also illustrated graphically in Figures 10 and Figures 11. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R2/R1 must be connected between the (+) plate of C_{OUT} and ground.
3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive V_{FB} node.
5. Keep the (-) plates of CIN and C_{OUT} as close as possible.



C_{FWD}: 22pF~220pF

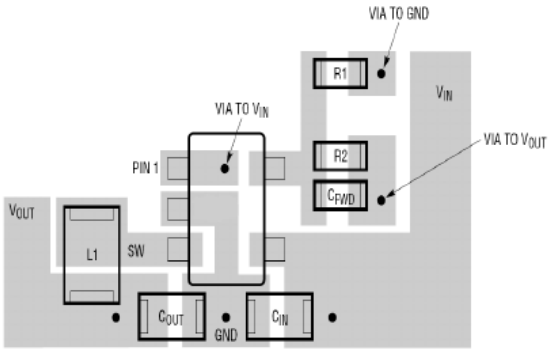
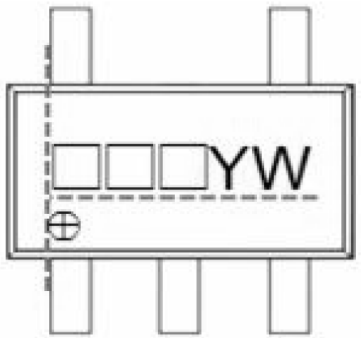


Figure 10: LSP5311 Adjustable Voltage Regulator Layout Diagram

Marking Information

(1) SOT-23-5L

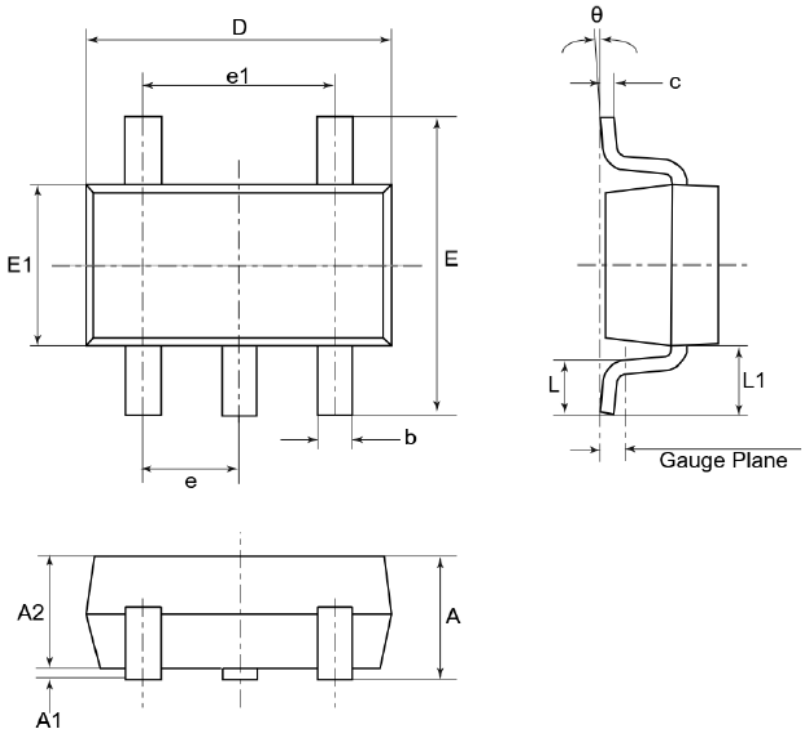


1) □□□ = Marking Name
(TBD) = LSP5311AAADADJ

2) YW = Date Code
Y = Year
W = Week

Mechanical Information

(2) SOT-23-5L



Unit: mm

Symbol	Min	Max
A	-	1.35
A1	-	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	2.60	3.00
E1	1.40	1.80
e	0.95 BSC	
e1	1.80	2.00
L	0.30	0.60
L1	0.60 REF	
Gauge Plane	0.25 REF	
θ	0°	8°

MSL (Moisture Sensitive Level) Information

IPC/JEDEC J-STD-020D.1 Moisture Sensitivity Levels Table

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			Standard		Accelerated Equivalent [1]		
					eV 0.40-0.48	eV 0.30-0.39	CONDITION
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	
1	Unlimited	≤30 ℃ /85% RH	168 +5/-0	85 ℃ /85% RH	NA	NA	NA
2	1 year	≤30 ℃ /60% RH	168 +5/-0	85 ℃ /60% RH	NA	NA	NA
2a	4 weeks	≤30 ℃ /60% RH	696[2] +5/-0	30 ℃ /60% RH	120 -1/+0	168 -1/+0	60 ℃/ 60% RH
3	168 hours	≤30 ℃ /60% RH	192[2] +5/-0	30 ℃ /60% RH	40 -1/+0	52 -1/+0	60 ℃/ 60% RH
4	72 hours	≤30 ℃ /60% RH	96[2] +2/-0	30 ℃ /60% RH	20 +0.5/-0	24 +0.5/-0	60 ℃/ 60% RH
5	48 hours	≤30 ℃ /60% RH	72[2] +2/-0	30 ℃ /60% RH	15 +0.5/-0	20 +0.5/-0	60 ℃/ 60% RH
a	24 hours	≤30 ℃ /60% RH	48[2] +2/-0	30 ℃ /60% RH	10 +0.5/-0	13 +0.5/-0	60 ℃/ 60% RH
6	Time on Label (TOL)	≤30 ℃ /60% RH	TOL	30 ℃ /60% RH	NA	NA	NA

Note 1: CAUTION - To use the ‘‘accelerated equivalent’’ soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the ‘‘standard’’ soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the ‘‘accelerated equivalent’’ may be used. Accelerated soak times may vary due to material properties (e.g .mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer’s exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor’s facility. If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 ℃/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 ℃/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours. If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 ℃/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 ℃/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.